

Effects of a Memristor in a Chaotic Circuit with Switching Oscillation States

Taishi Segawa, Yoko Uwate, and Yoshifumi Nishio

Dept. of Electrical and Electronic Engineering, Tokushima University,
2-1 Minami-Josanjima, Tokushima, Japan

Email: {segawa, uwate, nishio}@ee.tokushima-u.ac.jp

Abstract—We designed and simulated the chaotic circuit with the memristor. As a result, we obtained intermittency chaos in the proposed chaotic circuit using a memristor. Furthermore, we also investigated the mapping when the proposed chaotic circuit model can be defined simply.

I. INTRODUCTION

Chaos theory has attracted a great deal of attention from various fields and various applications have been proposed [1]–[3]. Chaos theory is expected to contribute to the future development of the information society and medicine.

Memristor is a nonlinear two-terminal circuit element [4]. This circuit element has attracted a great deal of attention because of this excellent resistance change characteristics by the history of the previous charge or flux flow through it [5], [6].

In our previous study, we found that a chaotic circuit with a memristor exhibited switching phenomena between periodic and chaotic oscillations [7].

In this study, we investigate attractors composed of the voltages and currents in original chaotic circuit and the charges that pass through the memristor to make clear the effect of the memristor.

II. MATERIALS AND METHOD

A. Memristor Mathematical Model

We use the *Hewlett-Packard* memristor model in the proposed chaotic circuit. The resistance value of the memristor is defined as memristance $M(q)$. The equation of $M(q)$ is given as in (1).

$$M(q) = \mu_v \frac{R_{\text{on}}^2}{D^2} q(t) + R_{\text{off}} \left(1 - \mu_v \frac{R_{\text{on}}}{D^2} q(t) \right) \quad (1)$$

B. Chaotic Circuit with the Memristor [7]

Figure 1(a) shows the proposed chaotic circuit with the memristor. The original chaotic circuit is the one shown in Fig. 1 with the memristor removed. Figure 1(b) shows the chaotic attractor of the proposed chaotic circuit.

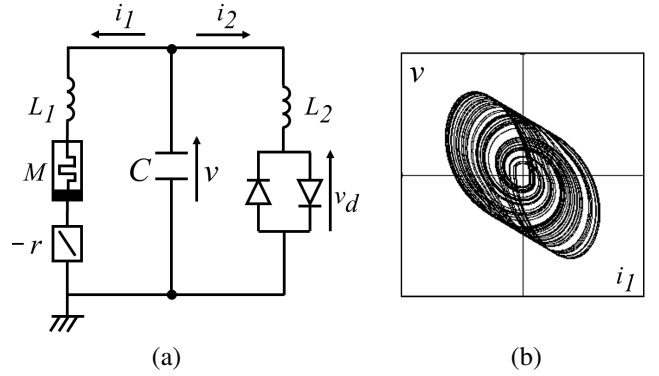


Fig. 1: Chaotic circuit model. (a) Proposed circuit model. (b) Chaos attractor.

The measured I - V characteristics of the diodes in the proposed chaotic circuit are approximated as follows:

$$v_d(i_2) = \frac{r_d}{2} \left(\left| i_2 + \frac{V}{r_d} \right| - \left| i_2 - \frac{V}{r_d} \right| \right) \quad (2)$$

The parameter r_d in (2) is the resistance value when the diodes are off state. The normalized circuit equations of the proposed circuit model in Fig. 1(a) is define as in (3).

$$\begin{cases} \dot{x} = z + \alpha x - \eta x (\zeta \xi w + 1 - \xi w) \\ \dot{y} = z - \frac{\gamma}{2} \left(\left| y + \frac{1}{\gamma} \right| - \left| y - \frac{1}{\gamma} \right| \right) \\ \dot{z} = -x - \beta y \\ \dot{w} = x \end{cases} \quad (3)$$

where τ is the scaling time, α is the negative resistance, β is the ratio of inductance, γ is the resistance of the nonlinear resistance when the diodes are off states, η is the maximum memristance, ξ is the minimum memristance, ζ is the ratio of maximum to minimum memristance.

III. RESULTS

In this study, the step size of the *Runge-Kutta* method $h = 0.002$. The parameters are set to $\tau = 10,000$, $\beta = 2.92$, $\gamma = 456$ and $\xi = 0.00276$. The parameters α , η and ζ are changed for each simulation condition.

A. Oscillation Switching Phenomena

In this subsection, the time-series of x , z , and w are investigated. Also, attractors on x - z plane are examined.

Figures 2 and 3 show examples of time-series waveforms and attractors.

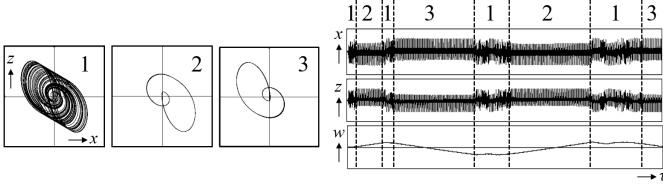


Fig. 2: 2-periodic and chaotic oscillations.

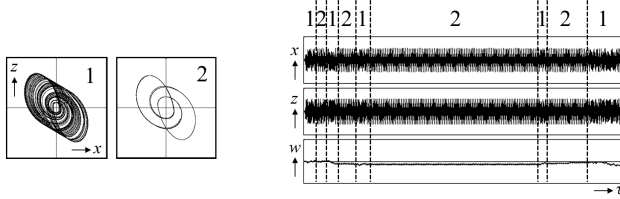


Fig. 3: 3-periodic and chaotic oscillations.

As shown in Figs. 2 and 3, we obtain oscillation switching phenomena between periodic and chaotic oscillations. This phenomena are new phenomena in the original chaotic circuit. Therefore, oscillation switching phenomena are arisen by adding the memristor. Table I summarize the switching combination and the simulation conditions that we obtained.

TABLE I: The switching combination.

	Oscillation Types
(a)	2-periodic, 5-periodic and chaotic oscillations
(b)	3-periodic and chaotic oscillations
(c)	7-periodic and chaotic oscillations
(d)	Multi-periodic and chaotic oscillations
(e)	Multi-periodic and chaotic oscillations

Table I shows the switching combination of each periodic and chaotic oscillations. As shown in Tab. I, five types of switching phenomena are observed.

B. Diodes are off-state

We investigate the dynamics at $y = 0$, it means the diodes of the nonlinear resistance are in the off state. Figure 4 shows attractors of x - z - w space and a mapping to x - w plane for 3-periodic and chaotic oscillations.

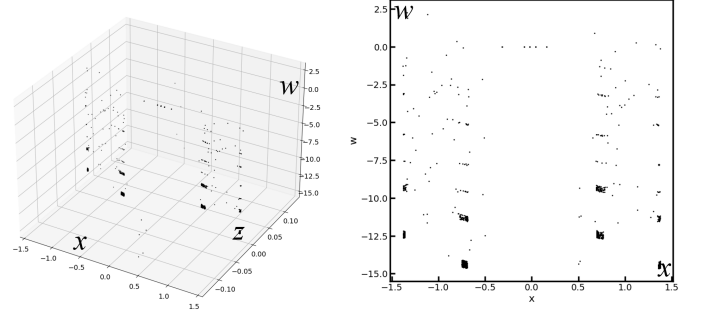


Fig. 4: Attractor and mapping for 3-periodic and chaotic oscillations

As shown in Fig. 4, the distribution of x is found to be different depending on the value of w . Therefore, we consider the dynamics of the memristor is the key to oscillation switching phenomena.

IV. CONCLUSIONS

This study designed and simulated the chaotic circuit with the memristor to analyzing the effect of the memristor in the chaotic circuit. We confirmed that the changes of x and z were limited, but the changes of w were significant than x and z . So, we considered the dynamics of the memristor is the key to the switching phenomena.

For the future work, we would like to investigate the mechanism of the oscillation switching phenomena in the proposed chaotic circuit model. In addition, we would like to design complex networks by using our proposed chaotic circuit using memristors for the future applications.

REFERENCES

- [1] Y. H. Ku, Xiaoguang Sun, "Chaos in van der Pol's Equation", Journal of the Franklin Institute, vol. 327, pp. 197-207, 1990.
- [2] S. Boccaletti, J. Kurths, G. Osipov, D. Valladares and C. Zhou, "The Synchronization of Chaotic Systems" Physics Reports, 366, pp. 1-101, 2002.
- [3] L. M. Pecora and T. L. Carroll, "Synchronization of Chaotic Systems," Chaos, vol. 25, 097611, <https://doi.org/10.1063/1.4917383>, 2015.
- [4] L. O. Chua, "Memristor-The Missing Circuit Element", IEEE Transactions on Circuit Theory, vol. CT-18, no. 5, pp. 507-519, September. 1971.
- [5] C. Yakopcic, T. Taha, G. Subramanyam, R. Pino and S. Rogers, "A Memristor Device Model", IEEE Electron Device Letters: Regular Paper, vol. 32, no. 10, pp. 1436-1438, September 2011.
- [6] Q. Geng, Y. Liang, Z. Lu, H. H-C. Iu and G. Wang, "Double Locally Active Memristor-Based Inductor-Free Chaotic Circuit, Proc. of 2024 IEEE International Symposium on Circuits and Systems (ISCAS), doi.10.1109/ISCAS58744.2024.10558563, July 2024.
- [7] T. Segawa, Y. Uwate and Y. Nishio, "Switching Phenomena by Adding a Memristor to a Chaos Circuit", Proc. of 2024 International SoC Design Conference (ISOCC'24), CS5-4 (2 pages), August 2024.
- [8] Y. Nishio, N. Inaba, S. Mori and T. Saito, "Rigorous Analyses of Windows in a Symmetric Circuit", IEEE Transactions on Circuit and Systems, vol. 37, no. 4, April 1990.