

# The Behavior of Chaotic Circuit Using Memristor in Series with Negative Resistance

Taishi Segawa, Yoko Uwate and Yoshifumi Nishio  
 Dept. of Electrical and Electronic Engineering, Tokushima University, Japan  
 2-1 Minami-Josanjima, Tokushima 770-8506, Japan  
 Email: {segawa, uwate, nishio}@ee.tokushima-u.ac.jp

**Abstract**—Combining chaos circuit and memristor may create realistic brain circuit in the future. Toward this realization, we would like to analyze the fundamental behavior of chaos circuit with one memristor in series. Therefore, we introduce new circuit equation and normalization parameter based on Nishio-Inaba chaos circuit to do computer simulations. We confirmed that memristor has a possibility to ease the strength of chaotic property and make a periodic solution by observing attractor and waveform. In addition, we also confirmed the amount of maximum and minimum memristance values can change the chaotic property of chaos circuit.

## I. INTRODUCTION

Memristor is a nonlinear electrical component that can change this resistance value  $M(q)$  depending on the amount of charge passing through it and magnetic flux linkage. Due to this property, memristor is considered as one of non-volatile storage technologies [1], [2], [3]. This memristor has attracted large attention as research topics and investigated some mathematical model like *Hewlett – Packard* model (HP model) and piecewise linear approximation model. These mathematical models are used for research about synchronization phenomena of electrical circuit, application for neural network, and so on [2].

Chaos is a random state of disorder and confusion. This phenomena has investigated for a long time in electronic engineering [4]. The behavior of chaos circuit can be applied to nonlinear phenomena in nature including human behavior. In recently, the chaos circuit with memristor has attracted to realize a brain circuit that implements a neural network and alternative human brain in circuit simulator [5].

In this paper, we analyse the behavior of one series memristor -based chaos circuit by observing attractor and waveform. Also, we analyse how does the memristance value  $M(q)$  affects the chaos circuit by changing the maximum and minimum memristance values.

## II. PROPOSED CIRCUIT MODEL

Figure 1 (a) shows the original Nishio-Inaba chaos circuit. This chaos circuit is consisted by three memory elements, one linear negative resistance and one nonlinear resistance consisting of two diodes. Fig. 1 (b) is proposed circuit model in this study that is added one memristor in original Nishio-Inaba circuit. One memristor  $M(q)$  is put into between inductor  $L_1$  and linear negative resistance  $-r$  in series.

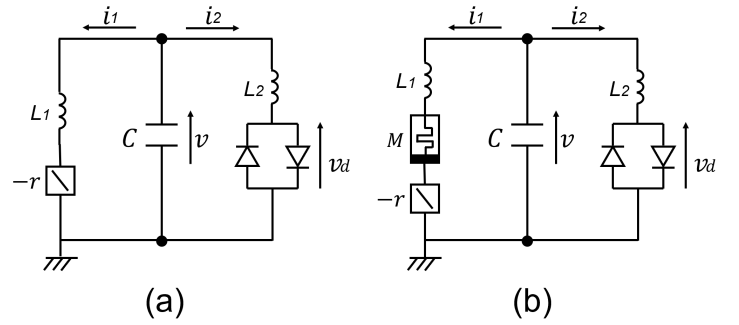


Fig. 1. Circuit model. (a) Original Nishio-Inaba chaos circuit. (b) Proposed one series memristor-based chaos circuit.

A memristor in proposed circuit model is defined as HP mathematical model to analyses the behavior of this circuit based on actual memristor value. The memristance  $M(q)$  of HP model is given as follows:

$$M(q) = R_{off} \left( 1 - \mu_v \frac{R_{on}}{D^2} q \right) \quad (1)$$

We approximate the  $I$ - $V$  characteristic by the piecewise-linear function as follows:

$$v_d(i_2) = \frac{r_d}{2} \left( \left| i_2 + \frac{V}{r_d} \right| - \left| i_2 - \frac{V}{r_d} \right| \right) \quad (2)$$

Then, the circuit equation of proposed model is described as follows:

$$\begin{cases} L_1 \frac{di_1}{dt} = v + r i_1 - M(q) i_1 \\ L_2 \frac{di_2}{dt} = v - v_d(i_2) \\ C \frac{dv}{dt} = -i_1 - i_2 \\ \frac{dq}{dt} = i_1 \end{cases} \quad (3)$$

By changing values such that

$$\begin{aligned}
i_1 &= \sqrt{\frac{C}{L_1}} Vx; & i_2 &= \frac{\sqrt{L_1 C}}{L_2} Vy; & v &= Vz; \\
q &= CVw; & t &= \sqrt{L_1 C}t; & r\sqrt{\frac{C}{L_1}} &= \alpha; \\
\frac{L_1}{L_2} &= \beta; & r_d\frac{\sqrt{L_1 C}}{L_2} &= \gamma; & R_{off}\sqrt{\frac{C}{L_1}} &= \eta; \\
\mu_v\frac{R_{on}}{D^2}CV &= \xi; & \text{".."} &= \frac{d}{d\tau}
\end{aligned} \tag{4}$$

(3) is normalized as

$$\begin{cases}
\dot{x} = z + \alpha x - \eta x(1 - \xi w) \\
\dot{y} = z - \frac{\gamma}{2} \left( \left| y + \frac{1}{\gamma} \right| - \left| y - \frac{1}{\gamma} \right| \right) \\
\dot{z} = -x - \beta y \\
\dot{w} = x
\end{cases} \tag{5}$$

In this paper, the values of two inductors  $L_1 = 603.2$  mH,  $L_2 = 206.5$  mH, capacitor  $C = 0.0069 \mu\text{F}$ , nonlinear resistor  $r_d = 1.46$  k $\Omega$ , and some memristance elements  $\mu_v = 10^{-14} \text{m}^2/\text{Vs}$ ,  $D = 10$  nm are fixed. When the value of one linear negative resistance  $r$  is variable to analyse the nonlinear property of proposed circuit model, memristance elements values  $R_{on}$  and  $R_{off}$  are fixed. On the other hand, when the values of memristance elements  $R_{on}$  and  $R_{off}$  are variable to analyse the influence of memristor for chaos circuit, one linear negative resistance  $r$  is fixed.

### III. SIMULATION RESULTS

#### A. Comparison of Proposed Circuit Model and Original Nishio-Inaba Circuit.

This section shows comparison results of proposed circuit model and standard Nishio-Inaba circuit model with fixed memristance values. The difference of attractors are shown in Fig. 2 (a), (b), (c), (d) and (e). The value of linear negative resistance  $-r$  differs under each patterns. In Fig. 2, left sides are attractors of proposed model and right sides are original Nishio-Inaba circuit attractors. In addition, the difference of waveform under each cases are shown in Fig. 3 (a), (b), (c), (d) and (e). These attractors and waveforms comes from the calculation results of Equation (5). Eq. (5) is calculated using Runge-Kutta method with the step size  $h = 0.02$  since  $\tau = 0$ .

From Fig. 2, it can be seen that the attractor becomes more complex as the value  $\alpha$  increases. Compare (b), (c) and (d) with proposed model (left sides) and original model (right sides), the original model has a solution curve that

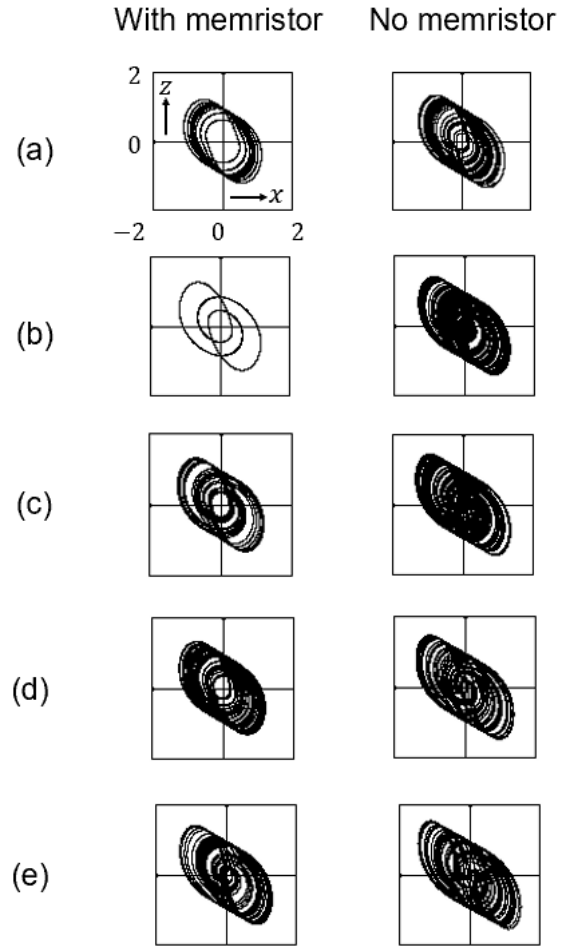


Fig. 2. The difference of attractor

(In case of with memristor,  $R_{on} = 10 \Omega$ ,  $R_{off} = 0.935 \text{k}\Omega$  ( $\mu = 0.100$ ,  $\xi = 6.90 \times 10^{-5}$ ))  
(a)  $r = 4.38 \text{k}\Omega \cdot \alpha = 0.468$ , (b)  $r = 4.82 \text{k}\Omega \cdot \alpha = 0.516$ ,  
(c)  $r = 5.07 \text{k}\Omega \cdot \alpha = 0.542$ , (d)  $r = 5.24 \text{k}\Omega \cdot \alpha = 0.560$ ,  
(e)  $r = 5.76 \text{k}\Omega \cdot \alpha = 0.616$ .)

passes near the origin, but the proposed model does not pass near the origin. Especially case (b), the solution curve is quite different. Original model has a chaos solution curve, but proposed model has a 3 period solution. From this simulation results, memristor has a possibility to ease the strength of chaotic property.

In Fig. 3, the axis scales of all graphs are the same except for Fig. 3 (e). The vertical axis scale for  $w$  of Fig. 3 (e) is 4 times larger than the others. From Fig. 3, a memristor remembers the amount of charge that has passed through it. So, the graph of  $w$  is linked to  $x$  that is equivalent to current  $i_1$  in Fig. 1 (b). And also can be seen that the waveform with no memristor is changed by adding memristor in series.

#### B. Influence of The Memristance Values for The Chaos Circuit

Here, the value of linear negative resistance is fixed and changing minimum resistance value  $R_{on}$  and maximum resistance value  $R_{off}$  to analyse influences of the memristance

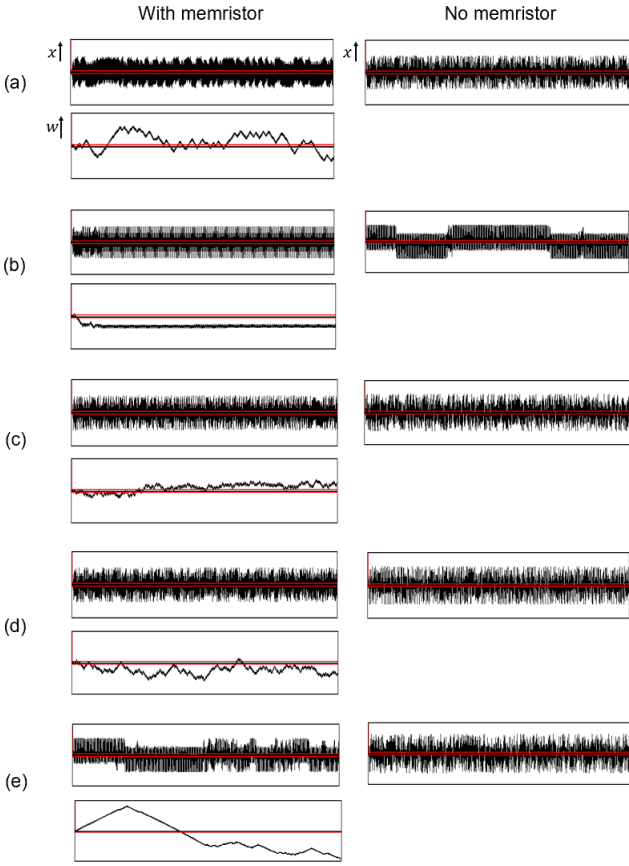


Fig. 3. The difference of waveform ( $R_{on} = 10 \Omega$ ,  $R_{off} = 0.935 \text{ k}\Omega$  and the vertical axis scale for  $w$  of (e) is 4 times larger than the others. ( $\mu = 0.100$ ,  $\xi = 6.90 \times 10^{-5}$ )  
(a)  $r = 4.38 \text{ k}\Omega \cdot \alpha = 0.468$ , (b)  $r = 4.82 \text{ k}\Omega \cdot \alpha = 0.516$ ,  
(c)  $r = 5.07 \text{ k}\Omega \cdot \alpha = 0.542$ , (d)  $r = 5.24 \text{ k}\Omega \cdot \alpha = 0.560$ ,  
(e)  $r = 5.76 \text{ k}\Omega \cdot \alpha = 0.616$ .)

values for this chaos circuit. Fig. 4 shows attractors when the value of  $R_{on}$  and  $R_{off}$  are gradually changed. Fig. 4 are using  $\alpha = 0.561$  that value is shown as a 3 period solution with memristor in Fig. 2 (b). The  $R_{on}$  and  $R_{off}$  values in each case are shown in Table I.

From Table I, the ratio of resistance  $R_{off}/R_{on} = 100$  is set to be almost constant. From Fig. 4, it can be seen that the chaotic attractor gradually becomes a periodic solution as the values of  $R_{on}$  and  $R_{off}$  increases. At first case (a), the attractor is observed as chaos attractor. This chaotic attractor becomes a 3 periodic solution attractor at case (e). After that case (e), this attractor gradually becomes a almost 1 periodic solution attractor at case (q). After case (q), the attractor has a chaotic property a little bit again. From these results, memristor has a possibility that it can ease the strength of chaotic property in a chaos circuit. However, increasing the values of  $R_{on}$  and  $R_{off}$  doesn't ease the strength of chaotic property definitely. Appropriate resistance values are necessary to ease the chaotic property in this simulation condition.

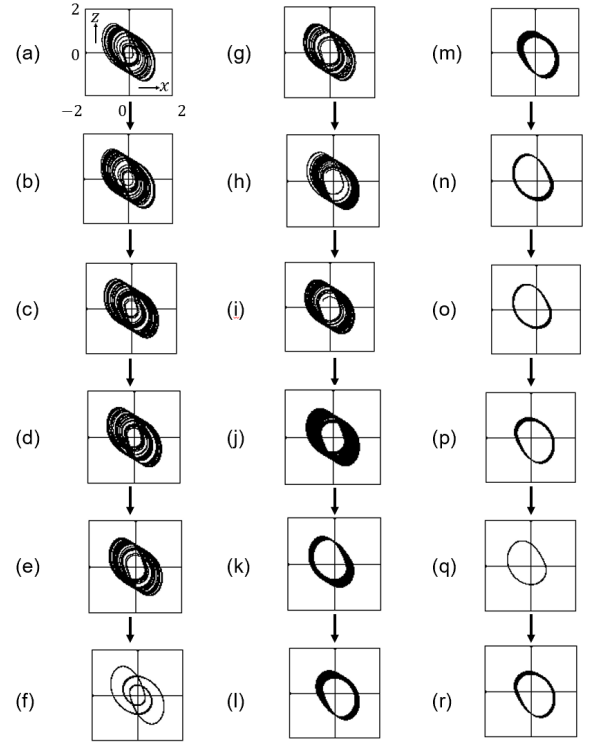


Fig. 4. Attractor change by each  $R_{on}$  and  $R_{off}$  values. ( $\alpha = 0.516$ )

TABLE I  
THE  $R_{on}$  AND  $R_{off}$  VALUES IN EACH CASE

	$R_{on} \Omega$	$R_{off} \text{ k}\Omega$	$\eta$	$\xi$
(a)	5	0.50	0.0535	$3.45 \times 10^{-5}$
(b)	6	0.60	0.0642	$4.14 \times 10^{-5}$
(c)	7	0.70	0.0749	$4.83 \times 10^{-5}$
(d)	8	0.80	0.0856	$5.52 \times 10^{-5}$
(e)	9	0.90	0.0963	$6.21 \times 10^{-5}$
(f)	10	0.935	0.100	$6.90 \times 10^{-5}$
(g)	10	1.00	0.107	$6.90 \times 10^{-5}$
(h)	11	1.10	0.118	$7.59 \times 10^{-5}$
(i)	12	1.20	0.128	$8.28 \times 10^{-5}$
(j)	13	1.30	0.139	$8.97 \times 10^{-5}$
(k)	14	1.40	0.150	$9.66 \times 10^{-5}$
(l)	15	1.50	0.160	$1.04 \times 10^{-4}$
(m)	16	1.60	0.171	$1.10 \times 10^{-4}$
(n)	17	1.70	0.182	$1.17 \times 10^{-4}$
(o)	18	1.80	0.193	$1.24 \times 10^{-4}$
(p)	19	1.90	0.203	$1.31 \times 10^{-4}$
(q)	20	2.00	0.214	$1.38 \times 10^{-4}$
(r)	21	2.10	0.225	$1.45 \times 10^{-4}$

#### IV. CONCLUSIONS

In this study, we proposed new chaos circuit model that is based Nishio-Inaba chaos circuit. One memristor is put into between a inductor  $L_1$  and one linear negative resistance  $-r$  in series. The behavior of this circuit model is investigated as seen attractor and waveform in each case that fixed the value of memristance elements  $R_{on}$  and  $R_{off}$  and fixed the value of a linear negative resistance  $-r$ . As a result, we discovered that the proposed circuit has a possibility to ease chaotic property and can became a periodic solution from chaotic solution. In attractor comparison with memristor circuit and no memristor circuit, the circuit with memristor give more periodic solution than no memristor one. Especially, in case of the circuit with no memristor gives a chaos solution, the circuit with memristor gives a 3 periodic solution expresses a possibility to ease chaotic property and can became a periodic solution from chaotic solution. In addition, a proposed circuit model can become a periodic solution from chaotic attractor gradually as the values of memristor elements  $R_{on}$  and  $R_{off}$  increases. It mean as increase the influence of memristor to chaos circuit by changing the values of memristance elements, we can adjustment the behavior of proposed circuit model as well as parameter  $\alpha$ .

For the future work, we would like to investigate the Nishio-Inaba circuit where one memristor and one liner negative resistance in parallel. We also would like to investigate the behavior of chaos circuit with other memristor mathematical model and other chaos circuit model.

#### REFERENCES

- [1] C. Yakopcic, T. Taha, G. Subramanyam, R. Pino and S. Rogers, " A Memristor Device Model ", IEEE Electron Device Letters: Regular Papers, vol. 32, no. 10, pp. 1436–1438, September 2011.
- [2] N. R. McDonald, R. E. Pino, P. J. Rozwood and B. T. Wysocki, "Analysis of dynamic linear and non-linear memristor device models for emerging neuromorphic computing hardware design", IEEE The 2010 International Joint Conference on Neural Network(IJCNN), no. 11594138, July 2010.
- [3] M. Escudero, S. Spiga, M. D. Marco, M. Forti, G. Innocenti, A. Tesi, F. Corinto and S. Brivio, "Chua's Circuit With Tunable Nonlinearity Based on a Nonvolatile Memristor: Design and Realization", IEEE Transactions on circuits and systems - I, Regular paper, pp. 1-11, 23 October 2023.
- [4] Y. Nishio, N. Inaba, S. Mori and T. Saito, " Rigous Analyses of Windows in a Symmetric Circuit ", IEEE Transactions on circuits and systems, vol. 37, no. 4, April 1990.
- [5] T. Tezuka, K. Kobayashi, Y. Uwate, Y. Hosokawa, Y. Nishio " Synchronization of Two Memristor-Based Chaotic Circuits Coupled by Resistor ", 2018 RIPS International Workshop on Nonlinear Circuits, Communications and Signal Processing (NCSP2018), March 2018.