17-60

A Spice-Oriented Designing Algorithm of Two-Stage CMOS Op-Amps

T. Ishikawa[1] Y. Yamagami[1] Y. Nishio[1] A. Ushida[2]
(Tokushima University[1] Tokushima Bunri University[2])

1. Introduction

In this study, we propose a Spice-oriented design algorithm of CMOS operational amplifiers, which is based on the steepest descent method. For attaining both the maximum gain and minimum power consumption, we need to set the suitable channel width of two-stage CMOS op-amps and the reference current as low as possible. The proposed algorithm whose circuit is realized by ABMs (Analog Behavior Models) of Spice. Firstly, we need to define the *objective function* as follow:

$$\Phi(\mathbf{x},\mathbf{p}), \quad \mathbf{x}\in R^n, \quad \mathbf{p}\in R^k \tag{1}$$

where
x: circuit variables such as voltages and currents.
p: optimization parameters such as channel width of CMOS and reference current and so on. The gradient direction is decided by the solutions of sensitivity circuits, and the steepest descent algorithm can be realized by the equivalent RC circuits combining with nonlinear controlled current sources.

2. Sensitivity modules of MOS

2.1 Sensitivity analysis: The steepest descent method is the most basic optimization approach, where the gradient direction is decided by the solutions of sensitivity circuit. The sensitivity circuit configuration is equal to the original one except for the nonlinear elements being replaced by controlled source.
2.2 Sensitivity modules of MOS transistor: For simplicity, we consider nMOS transistor modeled by Ebers-Moll model as shown in Fig.1. Fig.1(a) is sensitivity circuit module and Fig.1(b) is sensitivity circuit module with parameter variation.

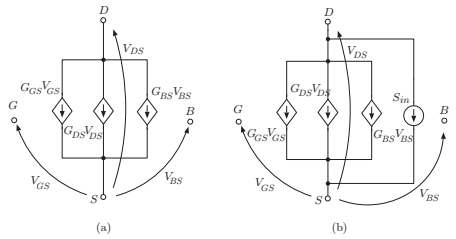

Fig. 1 Sensitivity modules of nMOS.

2.2.1 nMOS (the case element parameter is not change)

(a) linear region($V_{GS}>V_T, 0<V_{DS}<V_{GS}-V_T$)

$$G_{GS}\equiv\frac{\partial I_D}{\partial V_{GS}}=\frac{k_nW}{L}V_{DS}(1+\lambda V_{DS}) \tag{2}$$

$$G_{DS}\equiv\frac{\partial I_D}{\partial V_{DS}} =\frac{k_nW}{L}\left\{-\frac{3}{2}\lambda V_{DS}^2-V_{DS}+(1+2\lambda)(V_{GS}-V_T)\right\} \tag{3}$$

$$G_{BS}\equiv\frac{\partial I_D}{\partial V_{BS}}=\frac{\gamma k_nW}{2L}\frac{V_{DS}(1+\lambda V_{DS})}{\sqrt{\phi-V_{BS}}} \tag{4}$$

(b) saturated region($V_{GS}>V_T, V_{DS}\geq V_{GS}-V_T$)

$$G_{GS}\equiv\frac{\partial I_D}{\partial V_{GS}} = \frac{k_nW}{L}(V_{GS}-V_T)(1+\lambda V_{DS}) \tag{5}$$

$$G_{DS}\equiv\frac{\partial I_D}{\partial V_{DS}} = \frac{k_nW}{L}(V_{GS}-V_T)^2\lambda \tag{6}$$

$$G_{BS}\equiv\frac{\partial I_D}{\partial V_{BS}} = \frac{\gamma k_nW}{2L}\frac{(V_{GS}-V_T)(1+\lambda V_{DS})}{\sqrt{\phi-V_{BS}}} \tag{7}$$

2.2.2 a current source of nMOS sensitivity circuit with parameter variation$S_{in,L}, S_{in,W}$:

(a) linear region($V_{GS}>V_T, 0<V_{DS}<V_{GS}-V_T$)
a current source with variation of width W :

$$S_{in,W}=\frac{K_n}{L}\left\{(V_{GS}-V_T)-\frac{V_{DS}}{2}\right\}V_{DS}(1+\lambda V_{DS}) \tag{8}$$

(b) saturated region($V_{GS}>V_T, V_{DS}\geq V_{GS}-V_T$)
a current source with variation of width W :

$$S_{in,W}=\frac{k_n}{2L}(V_{GS}-V_T)^2(1+\lambda V_{DS}) \tag{9}$$

It is enable to consider pMOS similarly if you attend to direction of current.

3. Steepest descent method for attaining the maximum gain

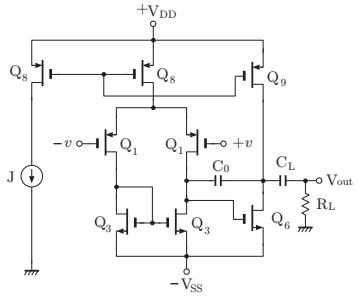

Fig. 2 Two-stage CMOS op-amps configuration.

Now, we consider Spice-oriented optimization technique for attaining the maximum gain of two-stage CMOS op-amps. We need to introduce the numerical differentiation technique for the optimization of the gain, because the gain is obtained by the sensitivity circuit. The gradient for attaining the maximum gain is given by

$$\frac{dp_i}{ds}=-\frac{dS_v(\mathbf{p})}{dp_i}, \quad i=1,2,\cdots,k, \tag{10}$$

where $S(\mathbf{p})$ is the gain, and p is optimization parameter. Unfortunately, it is impossible directly to evaluate $\frac{dS(p)}{dp_i}$ from the sensitivity analysis, so that we introduce the *numerical differentiation* as follows;

$$\frac{dp_i}{ds}=-\frac{S_{v,i}(\mathbf{p}+\Delta\ \mathbf{p})-S_v(\mathbf{p})}{\Delta\ p_i}, \quad i=1,2,\cdots,k, \tag{11}$$

$$\Delta\ \mathbf{p}=(0,0,\cdots,\Delta\ p_i,\cdots,0)^T$$

with sufficiently small $\Delta\ \mathbf{p}$. Replacing the auxiliary variable "s" by time "t", our descent algorithm can be realized by the equivalent nonlinear RC circuits, and the optimum parameters can be found by equilibrium point of the transient analysis. We get the following result; when the minimum current is set to 50 [μA], we attained the maximum gain = −20.4.

4. Conclusions and remarks

In this study, we proposed a Spice-oriented designing algorithm of two-stage CMOS op-amps, the optimization technique is based on the steepest descent method, whose gradient is calculated by the sensitivity circuits. The equivalent steepest descent circuit consists of ABMs of Spice, and the optimum point can be found by the solution of the transient analysis. This conclusion provide us to use CMOS more practically.

References

[1] A. Ushida and M. Tanaka, *Electronic Circuit's Simulations,* Korona Pub. Co., 2002 (Japanese).