

Effect of Memristance Change on Oscillation Switching in a Chaotic Circuit

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Abstract—We design and investigate a four-dimensional chaotic circuit with a memristor by adding a Hewlett-Packard memristor to a Nishio-Inaba chaotic circuit. From the circuit, we observe interesting oscillation switching of periodic and chaotic oscillations over time. Such oscillation switching phenomena are not observed from the original chaotic circuit. We investigate the phenomena by the detailed analysis by changing the range of resistance value of the memristor.

1. Introduction

Chaos has a nonlinear nature in which small differences in initial values expand exponentially into the future, making long-term predictions difficult. Chaos is attracting a great deal of attention because this nonlinearity is expected to deepen our understanding of nonlinear science and to have engineering applications. One of the most famous applications is the chaotic neural network. The chaotic property of neuron has been reported to make it possible to extract features and form associative memories using various spatiotemporal patterns [1]. However, these neural networks are implemented by digital computers due to their complex structure. Digital computers cannot handle real numbers with infinite digits, and there are limitations to reproducing brain functions. Furthermore, complex structures have the problem of making the processing in the intermediate layer a black box. For this reason, it is expected that chaotic information processing will be realized with analog devices. Therefore, chaotic circuits are one of the effective means. Furthermore, analog memory elements that can handle infinite digits are also attracting attention. In this study, we focused on a memristor.

A memristor which was introduced by L. O. Chua in 1971 is a nonlinear two-terminal circuit element [2]. Also, it was developed by *Hewlett-Packard* laboratory in 2008. This circuit element has attracted a great deal of attention because of the excellent resistance change characteristics by the history of the charge or flux flow through it

[3, 4]. Therefore, researchers are investigating the electrical characteristics of memristors themselves and the impact of memristors on electrical circuits[5].

In this study, we designed a chaotic circuit with a memristor. We investigated the dynamics of the circuit by observing orbits on phase planes and time-series waveforms. In addition, we investigated the behavior of the circuit by changing the range of resistance value of the memristor.

2. Materials and Methods

2.1. Memristor model

By using the memristor, we can realize a chaotic circuit with an additional function to store the history of charge that passes through as nonlinear and analog resistance change. In this study, we adopt the Hewlett-Packard memristor model. Figures 1(a) and (b) show a schematic symbol and v - i characteristics. When a sine wave is input, the v - i characteristics become a pinched hysteresis loop.

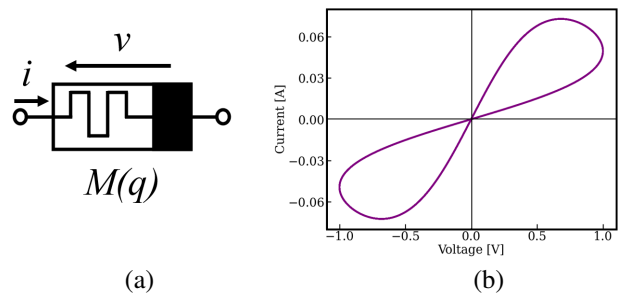


Figure 1: Memristor model. (a) Schematic symbol. (b) v - i characteristics (Amplitude and frequency of the input are 1 V and 1 kHz).

The resistance of the memristor is defined as memristance $M(q)$ and is described as a function of the passing charge $q(t)$ in (1).

$$M(q) = \mu_v \frac{R_{\text{on}}^2}{D^2} q(t) + R_{\text{off}} \left(1 - \mu_v \frac{R_{\text{on}}}{D^2} q(t) \right). \quad (1)$$

where R_{on} is the minimum memristance, R_{off} is the maximum memristance, μ_v is the average drift mobility of the charges, and D is the length of doped and undoped parts.

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2.2. Chaotic circuits with memristors

We construct the chaotic circuit with the memristor shown in Fig. 2. This circuit is the four-dimensional autonomous circuit. We adopt the Nishio-Inaba circuit as the base chaotic circuit. Nishio-Inaba circuit consists of one negative resistor r , one capacitor C , two inductors L_1 and L_2 , and one dual-directional diodes. As a feature of Nishio-Inaba circuit, i_1 in Fig. 2 becomes larger than i_2 when chaotic oscillation is observed. To increase effects of adding the memristor in the based circuit, we add the memristor between L_1 and r in series.

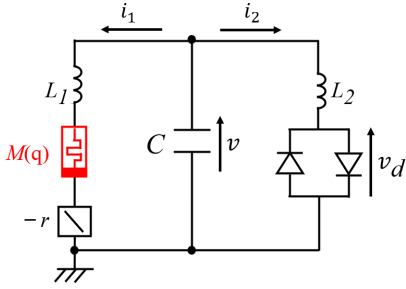


Figure 2: Chaotic circuit with the memristor.

When two coupled circuits, each circuit is coupled via a pure resistor R shown in Fig. 3.

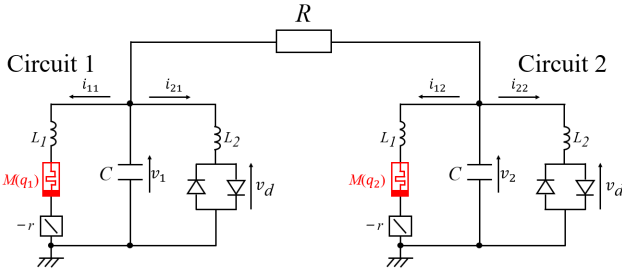


Figure 3: Two coupled chaotic circuits with memristors.

The v - i characteristics of the dual-directional diodes in Figs. 2 and 3 are approximated as the three-segment piecewise-linear function defined in (2). The parameter r_d is resistance when the diodes are off and V is the threshold voltage of the diodes.

$$v_d(i_2) = \frac{r_d}{2} \left(\left| i_2 + \frac{V}{r_d} \right| - \left| i_2 - \frac{V}{r_d} \right| \right). \quad (2)$$

By using the variables and the parameters,

$$i_{1n} = \sqrt{\frac{C}{L_1}} V x, \quad i_{2n} = \frac{\sqrt{L_1 C}}{L_2} V y, \quad v_n = V z, \quad q_n = C V w,$$

$$t = \sqrt{L_1 C} \tau, \quad \cdot \cdot \cdot = \frac{d}{d\tau}, \quad r \sqrt{\frac{C}{L_1}} = \alpha, \quad \frac{L_1}{L_2} = \beta,$$

$$r_d \frac{\sqrt{L_1 C}}{L_2} = \gamma, \quad R_{\text{off}} \sqrt{\frac{C}{L_1}} = \eta, \quad \frac{R_{\text{on}}}{R_{\text{off}}} = \zeta, \quad \mu_v \frac{R_{\text{on}}}{D^2} C V = \xi,$$

the normalized circuit equations are given as follows:

$$\begin{cases} \dot{x}_n = z_n + \alpha x_n - \eta x_n (\zeta \xi w_n + 1 - \xi w_n) \\ \dot{y}_n = z_n - \frac{\gamma}{2} \left(\left| y_n + \frac{1}{\gamma} \right| - \left| y_n - \frac{1}{\gamma} \right| \right) \\ \dot{z}_n = -x_n - \beta y_n - \sum_{k=1}^n \delta (z_n - z_k) \\ \dot{w}_n = x_n \end{cases} \quad (3)$$

$(n = 1, 2).$

where α is the negative resistance, β is the ratio of inductance, γ is the resistance of the nonlinear resistor when the diodes are off, η is the maximum memristance, ζ is the minimum memristance, ξ corresponds to the average drift mobility of the charges, and δ is the resistance value connecting the circuits. The important point of (3) is the $\eta x (\zeta \xi w + 1 - \xi w)$ term. The $\eta x (\zeta \xi w + 1 - \xi w)$ term corresponds to current and memristance. Due to the generation of this product term, new nonlinear phenomena are expected to be observed.

In the computer calculation, the step size of the Runge-Kutta method is set to $h = 0.002$. This numerical calculation is performed for τ from 0 to 10,000. All parameters except ζ are fixed to $\alpha = 0.588$, $\beta = 2.92$, $\gamma = 456$ and $\xi = 0.00276$. The initial value of the variable varies randomly between -0.0600 and 0.0600 .

3. Oscillation switching phenomena

The purpose of this section is observing new complex behavior in the based chaotic circuit by adding the memristor. As a result, we confirm the oscillation switching phenomenon of periodic and chaotic oscillations over time in single circuit and two coupled circuits. In the case of the Nishio-Inaba circuit, we can observe either periodic or chaotic oscillations during the circuit is running. Thus, these oscillation switching phenomena over time are new caused by adding a memristor to the Nishio-Inaba circuit. Figures 4 shows a example of oscillation switching phenomena with $\zeta = 0.126$. This is the oscillation switching of 2-periodic and chaotic oscillations.

In Fig. 4, a point symmetric 2-periodic oscillations are denoted by "A" and "B", while the chaotic oscillation is denoted by "C". From orbits on x - z plane and time-series waveform in Fig. 4, it can be seen that periodic and chaotic oscillations alternate. In addition, the behavior of w is completely different from x and z . According to (3), the behavior of w is related to the change of memristance. So, we consider the change of memristance is the key of oscillation switching phenomena. To investigate how the behavior of the memristor contributes to oscillation switching, we need to tune the influence of the memristor on the chaotic circuit. Thus, we focus on the parameter ζ . From the definition of ζ , it is related to the resistance difference of maximum and

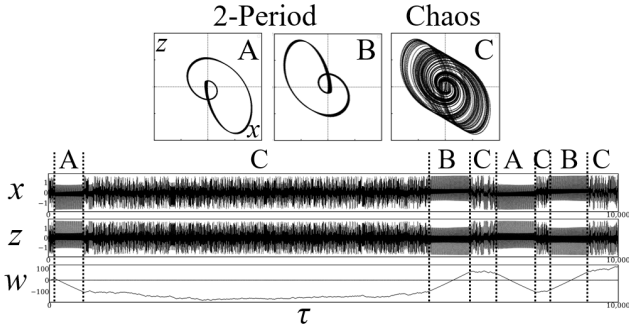


Figure 4: Oscillation switching of 2-periodic and chaotic oscillations in single circuit.

minimum memristance. So when ζ is set as 1.0, it is the same as a pure resistor. It indicates that we can tune ratio of maximum and minimum memristance. In next section, we investigate whether switching occurs, the ratio of periodic and chaotic oscillations during the circuit running, the number of switching events, and phase differences in the coupled circuit associated with changes in ζ .

4. Behavior of the circuit by changing ζ

The purpose of this section is to analyze the effect of the memristance difference of maximum and minimum on the oscillation switching. In this section, ζ varies from 1.0 to 0.1 by 0.05.

4.1. Ratio of periodic and chaotic oscillations

Figure 5 shows the change of the ratio of chaotic oscillations by changing ζ . The ratio of chaotic oscillations at each ζ is the average value obtained by setting 5 different initial values.

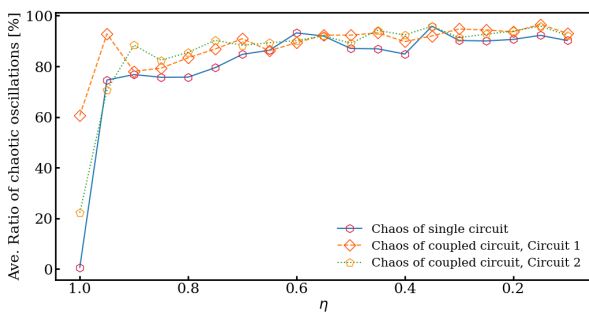


Figure 5: Ratio of chaotic oscillations.

From Fig. 5, we can see that there is almost no chaotic oscillation at $\zeta = 1.0$. However, at $\zeta = 0.95$, the distribution of chaotic oscillations changes rapidly to become more prevalent than periodic oscillations. After that, as ζ becomes smaller, that is, as the difference between the maximum and minimum values of memristance becomes larger, the proportion of chaotic oscillations gradually increases.

4.2. Number of switching events

Figure 6 shows the change of the number of oscillation switching events associated with changes in ζ . The number of oscillation switching events at each ζ is the average value obtained by setting 5 different initial values.

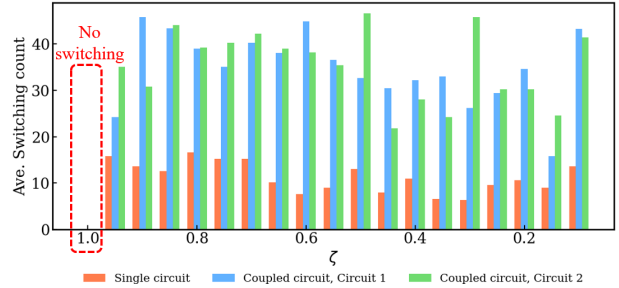


Figure 6: Number of switching events.

From Fig. 6, we can see that the oscillation switching does not occur at $\zeta = 1.0$. However, it can be seen that the oscillation switching occurs when ζ takes a value less than 1, i.e., when a memristance difference with a maximum and minimum value is created in the memristor. Furthermore, Fig. 7 shows the v - i characteristics of the memristor in the chaotic circuit before and after oscillation switching occurs in Fig. 6.

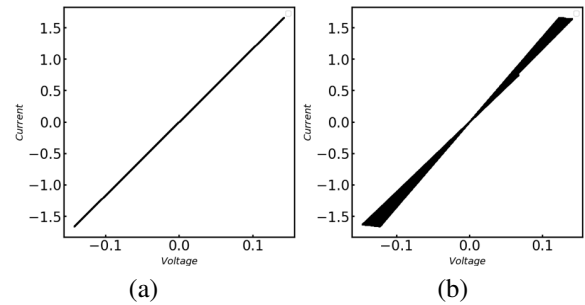


Figure 7: v - i characteristics of the memristor. (a) $\zeta = 1.0$. (b) $\zeta = 0.95$.

From Figs. 7(a) and (b), before the oscillation switching occurs ($\zeta = 1.0$), the v - i characteristic of the memristor is linear and closely resembles the v - i characteristic of a pure resistor. After switching occurs ($\zeta = 0.95$), the v - i characteristic of the memristor is found to be nonlinear with a wide range than the v - i characteristic at $\zeta = 1.0$. In other words, the condition for oscillation switching to occur is the presence of a maximum and minimum resistance difference in the memristor.

In addition, even for ζ where the ratio of periodic to chaotic oscillations is almost the same as in Fig. 5, the coupled circuit has more switching events than the single circuit. Furthermore, the number of oscillation switching events is distributed without being significantly dependent on the ζ . In other words, the memristance range does not have a significant relationship to the number of oscillation

switching events, but the existence of a range of memristance is confirmed to be closely related to the occurrence of switching itself.

4.3. Phase differences

In the coupled circuit, we investigated how the phase difference changes by changing ζ . The phase difference is calculated using the Poincaré map. The Poincaré section is defined as the region $H \subset x > 0, z = 0$. When "Circuit 1" in Fig. 3 passes through the Poincaré section, the phase difference between "Circuit 1" and "Circuit 2" is calculated. The result is shown in Fig. 8.

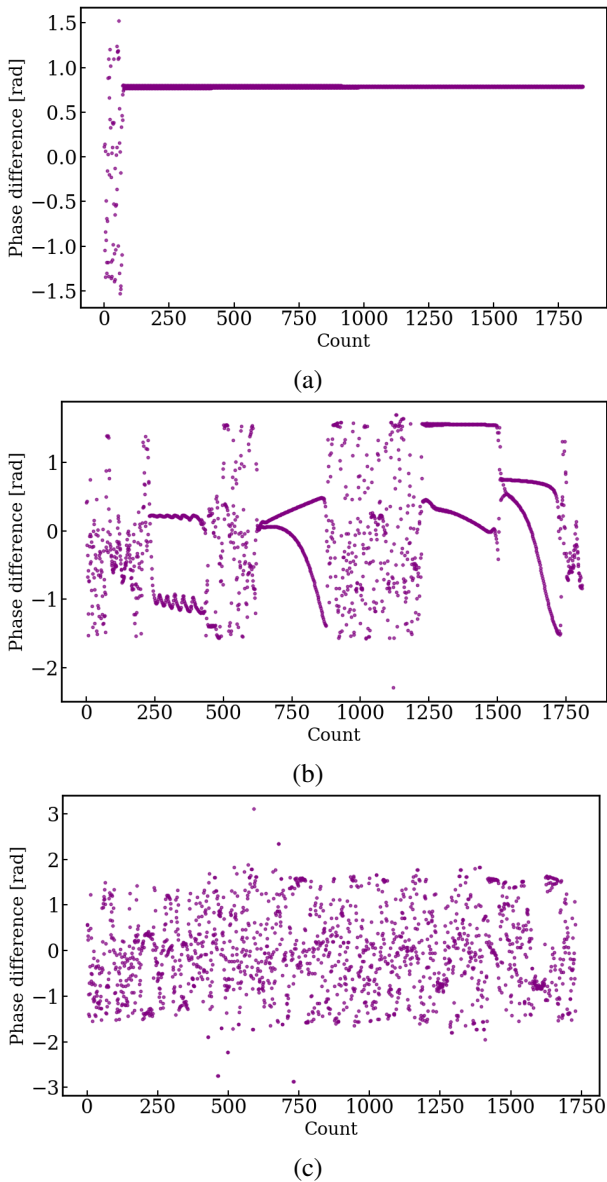


Figure 8: Phase differences. (a) $\zeta = 1.0$. (b) $\zeta = 0.95$. (c) $\zeta = 0.10$.

As shown in Fig.8(a), when $\zeta = 1.0$, the phase difference remains nearly constant and stable, indicating that each os-

cillator exhibits periodic oscillation. However, as shown in Fig.8(b), when $\zeta = 0.95$, intervals of constant phase difference alternate with intervals of varying phase difference. During the constant intervals, periodic oscillations are observed, whereas during the varying intervals, the oscillations become chaotic. Furthermore, as shown in Fig. 8(c), when $\zeta = 0.10$, the phase difference is distributed over a wide range with almost no intervals of constancy. In this case, each oscillator exhibits fully chaotic behavior.

5. Conclusions

In this study, we designed a chaotic circuit with a memristor. We investigated the dynamics of the circuit by observing orbits on phase planes and time-series waveforms. We confirmed the oscillation switching phenomenon of periodic and chaotic oscillations over time. In addition, we investigated the behavior of the circuit by changing ζ . As a result, the condition for oscillation switching to occur is the presence of a maximum and minimum resistance difference in the memristor. We also confirmed that the oscillation state and phase difference of each oscillator can be changed by adjusting the coupling strength in the coupling circuit.

Acknowledgments

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References

- [1] W. Lin and G. Chen, "Large Memory Capacity in Chaotic Artificial Neural Networks: A View of the Anti-Integrable Limit", *IEEE Transactions on Neural Networks*, vol. 20, no. 8, pp. 1340-1351, doi:10.1109/TNN.2009.2024148, July 2009.
- [2] L. O. Chua, "Memristor-The Missing Circuit Element", *IEEE Transactions on Circuit Theory*, vol. CT-18, no. 5, pp. 507-519, September. 1971.
- [3] C. Yakopcic, T. Taha, G. Subramanyam, R. Pino, and S. Rogers, "A Memristor Device Model", *IEEE Electron Device Letters: Regular Paper*, vol. 32, no. 10, pp. 1436-1438, 2011.
- [4] Q. Geng, Y. Liang, Z. Lu, H. H-C. Iu, and G. Wang, "Double Locally Active Memristor-Based Inductor-Free Chaotic Circuit", *Proc. of 2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, doi:10.1109/ISCAS58744.2024.10558563, 2024.
- [5] F. Corinto, M. Gilli, and M. Forti, "Flux-Charge Description of Circuits With Non-Volatile Switching Memristor Devices", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 5, pp. 642-646, doi:10.1109/TCSII.2018.2825447, 2018.