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Switching Phenomena by Adding a Memristor to a Chaos Circuit

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Abstract— **Coupled chaotic circuit and memristor has a possibility to create realistic brain circuit and replace AI algorithm which is realized by computer program codes in the future. In order to realize them, we propose a new chaotic circuit model using a memristor which the resistance value can be changed in analog and investigate fundamental behavior of the proposed circuit model by computer simulation. We found that switching phenomena between chaotic and periodic oscillations over time occurred by adding a memristor in a chaotic circuit.**

Keywords; Chaos, Oscillatior, Memristor, Switching

I. INTRODUCTION

In recent years, a memristor which was invented by Leon Chua in 1971 has attracted large attention as research topics and investigated their fundamental property and mathematical model such as *Hewlett-Packard* (HP) model and piecewise linear approximation model. Memristor is a nonlinear circuit element which can change this resistance value *M(q)* depending on the amount of charge passing through it. Due to this property, memristor is recognized as one of a non-volatile storage technology [1], [2].

Chaotic circuits are excellent models for describing some nonlinear phenomena occurring in our living world. In particular, chaotic and periodic oscillations due to changes in parameter values are an important model that suggests that the state of nonlinear phenomena can change from dynamic to static one.

In our research group, we consider coupled chaotic circuit and memristor has a possibility to reproduce a part of human brain function in the future. Some research investigated the dynamics of coupled circuits model using a piecewise linear approximation memristor model. So, we focus on an analog value-changing memristor model and add it to a chaotic circuit based on Nishio-Inaba chaotic circuit.

II. MEMRISTOR MATHEMATICAL MODEL

HP model can change this resistance value called memristance $M(q)$ by the amount of charge that is in a memristor in analog. Equation (1) is the definite expression of $M(q)$

$$M(q) = \mu\frac{\mathrm{R}_{\mathrm{on}}^2}{\mathrm{D}^2}q + \mathrm{R}_{\mathrm{off}}\left(1-\mu\frac{\mathrm{R}_{\mathrm{on}}^2}{\mathrm{D}^2}q\right) \tag{1}$$

μ is mobility, D is the length of this model, $\mathrm{R_{on}}$ is the minimum resistance value and $\mathrm{R_{off}}$ is the maximum resistance value.

III. PROPOSED CIRCUIT MODEL

Figure 1(a) is a proposed circuit model. A memristor is added between inductor $\mathrm{L_1}$ and negative resistor r in series. We approximate the $I – V$ characteristic of a nonlinear resistor by the piecewise linear function as follows:

$$v_d(i_2)=\frac{\mathrm{r_d}}{2}\left(\left|i_2+\frac{V}{\mathrm{r_d}}\right| - \left|i_2-\frac{V}{\mathrm{r_d}}\right|\right) \tag{2}$$

Then, the normalized circuit equation is defined as follows:

$$\begin{cases}\dfrac{\mathrm{d}x}{\mathrm{d}\tau} = \alpha x + z - \eta x(\zeta\xi w + 1 - \xi w) \\ \dfrac{\mathrm{d}y}{\mathrm{d}\tau} = z - \dfrac{\gamma}{2}\left(\left|y+\dfrac{1}{\gamma}\right| - \left|y-\dfrac{1}{\gamma}\right|\right) \\ \dfrac{\mathrm{d}z}{\mathrm{d}\tau} = -x-\beta y \\ \dfrac{\mathrm{d}w}{\mathrm{d}\tau} = x\end{cases} \tag{3}$$

with

$$i_1 = \sqrt{\frac{\mathrm{C}}{\mathrm{L_1}}}Vx,\quad i_2 = \frac{\sqrt{\mathrm{L_1C}}}{\mathrm{L_2}}Vy,\quad v=Vz,\quad q=\mathrm{C}Vw,\quad \mathrm{t}=\sqrt{\mathrm{L_1C}}\tau,$$

$$\mathrm{r}\sqrt{\frac{\mathrm{C}}{\mathrm{L_1}}}=\alpha,\ \frac{\mathrm{L_1}}{\mathrm{L_2}}=\beta,\ \mathrm{r_d}\frac{\sqrt{\mathrm{L_1C}}}{\mathrm{L_2}}=\gamma,\ \mathrm{R_{off}}\sqrt{\frac{\mathrm{C}}{\mathrm{L_1}}}=\eta,$$

$$\frac{\mathrm{R_{on}}}{\mathrm{R_{off}}}=\zeta,\ \mu\frac{\mathrm{R_{on}}}{\mathrm{D}^2}\mathrm{C}V=\xi$$

In Fig. 1(b), we put a capacitor $\mathrm{C_2}$ at the memristor location which capacitance is smaller than $\mathrm{C_1}$ so that we set the circuit equation as the same number of dimensions with Eq. (3). The normalized circuit equation is defined as follows:

$$\begin{cases}\dfrac{\mathrm{d}x}{\mathrm{d}\tau} = \beta x - z + w \\ \dfrac{\mathrm{d}y}{\mathrm{d}\tau} = \alpha_{\mathrm{L}}\left\{w - \dfrac{\left|\frac{y}{\varepsilon}+1\right| - \left|\frac{y}{\varepsilon}-1\right|}{2}\right\} \\ \dfrac{\mathrm{d}z}{\mathrm{d}\tau} = \alpha_{\mathrm{C}}x \\ \dfrac{\mathrm{d}w}{\mathrm{d}\tau} = -x-y\end{cases} \tag{4}$$

with

$$i_1 = \sqrt{\frac{\mathrm{C_2}}{\mathrm{L_1}}}Vx,\quad i_2 = \sqrt{\frac{\mathrm{C_2}}{\mathrm{L_1}}}Vy,\quad v_1 = Vz,\quad v_2 = Vw,\quad t=\sqrt{\mathrm{L_1C_2}}\tau,$$

$$\alpha_{\mathrm{C}} = \frac{\mathrm{C_1}}{\mathrm{C_2}},\quad \alpha_{\mathrm{L}}=\frac{\mathrm{L_1}}{\mathrm{L_2}},\quad \beta=\mathrm{r}\sqrt{\frac{\mathrm{C_2}}{\mathrm{L_1}}},\quad \varepsilon=\frac{1}{\mathrm{r_d}}\sqrt{\frac{\mathrm{L_1}}{\mathrm{C_2}}}$$

The difference between Eq. (3) and Eq. (4) is that Eq. (3) has a variable times variable term like "$\eta\, x(\zeta\xi w+1—\xi w)$". This term is an important element in this proposed circuit model.

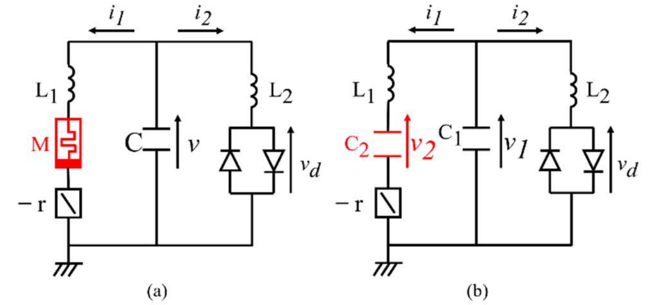

Figure 1. Circuit model. (a) Nishio-Inaba circuit using a memristor and (b) Nishio-Inaba circuit using a small capacitor.

In our simulation, the step size h of Runge-Kutta is set to h=0.002. Also, we can change α, η, ζ in Eq. (3) and parameters other than β in Eq. (4).

IV. SIMULATION RESULTS

A. *Nishio-Inaba Circuit with a Memristor*

In this section, we investigate behavior of Fig. 1(a) model by changing α, η, ζ values. We found new phenomena in a Nishio-Inaba chaotic circuit. They are switching phenomena. The behavior of these phenomena are switching between chaotic and periodic oscillations over time. These switching phenomena do not happen in the original Nishio-Inaba chaotic circuit. Also, we found the number of periodic orbits and switchcover time between chaotic and periodic oscillations depends on parameters setting. Figure 2 is one example of attractors and waveforms when the switching between two-periodic and chaotic oscillations occurred. Also, Fig. 3 is three-periodic and chaotic oscillations switching. Table 1 shows all patterns when switching occurred. Switching phenomena were confirmed 30 patterns out of 96 patterns. Especially, one-period switching occurred on 4 patterns, two-period switching is 15 patterns, three-period switching is 4 patterns and multi-period switching is 7 patterns. Others are only chaotic or periodic oscillations throughout the simulation time.

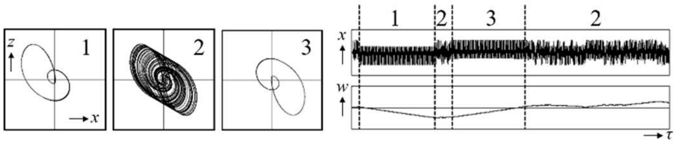

Figure 2. Switching of two-periodic and chaotic oscillations.

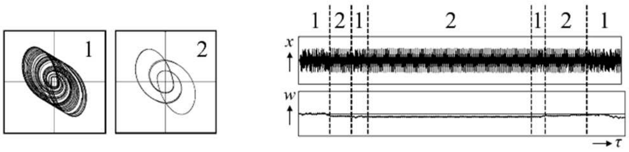

Figure 3. Switching of three-periodic and chaotic oscillations.

Table 1. Switching states of Fig. 1(a) model.

🔵 One-period switching 🔴 Two-period switching 🟢 Three-period switching ⚫ Multi-period switching

η	ζ	α 0.333	0.468	0.524	0.542	0.560	0.588	0.616	0.627
0.428	0.0250								
0.321	0.0333					🔵		🔵	🔵
0.214	0.0500		🔵	🔵					🟢
0.107	0.100		🔵		🟢			🔴	
0.0963	0.111		⚫	🟢			🔴	🔴	
0.0856	0.125		⚫				🔴		
0.0749	0.143					🔴	🔴		
0.0642	0.167					🔴	🔴		
0.0535	0.200				🔴	🔴		⚫	
0.0428	0.250		🟢	🔴	🔴				
0.0321	0.333		⚫	🔴	🔴				
0.0214	0.500		⚫	🔴			⚫		

B. *Nishio-Inaba Circuit with a Small Capacitor*

In this section, we investigate behavior of Fig. 1(b) model by changing $\alpha_{C,}$ α_L and ξ. We find that not only chaotic or periodic oscillations observed as well as in standard Nishio-Inaba circuit, but also super multi-periodic oscillations as shown in Fig. 4 are observed. However, the switching phenomena that is observed in Fig. 1(a) model are not observed with any parameters setting in Fig. 1(b).

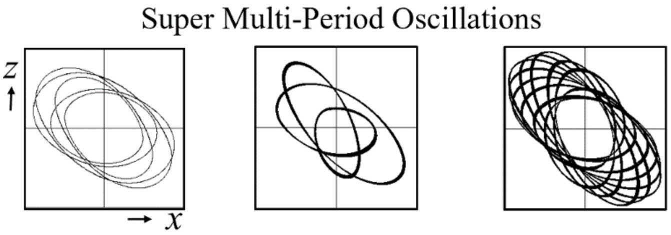

Figure 4. Oscillation states of Fig. 1(b) model.

This result suggests that the switching phenomena between chaotic and periodic oscillations are not caused simply by increasing the dimension of the circuit equations. We consider the switching phenomena come from the addition a memristor to a chaotic circuit, and the lager difference between Eq. (3) and Eq. (4) is that Eq. (3) has a variable multiplication term.

V. CONCLUSION

In this study, we have proposed a new chaotic circuit based on Nishio-Inaba chaotic circuit using *Hewlett-Packard* memristor model. To compare the features of this proposed circuit, we also have proposed a chaotic circuit based on Nishio-Inaba chaotic circuit using a small capacitor. We have confirmed that proposed circuit using a memristor could occur the switching phenomena of chaotic and periodic oscillation over time. In addition, the number of periodic orbits can be changed by the value of α and maximum resistance value of a memristor $R_{off.}$

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