2007 International Symposium on Nonlinear Theory and its Applications
NOLTA'07, Vancouver, Canada, September 16-19, 2007

Spice-Oriented Optimization Algorithm of Amplifiers - Based on Nonlinear Programing -

Akio Ushida†, Junji Kawata†, Yoshihiro Yamagami‡, Yoshifumi Nishio‡
†Department of Mechanical and Electronic Engineering,
Tokushima Bunri University, Kagawa, 769-2193 JAPAN
‡Department of Electrical and Electronic Engineering,
Tokushima University, Tokushima, 770-8506 JAPAN

Abstract

We propose an efficient Spice-oriented design algorithm of amplifies for attaining both the DC maximum gains and the low power consumptions. Our optimization algorithm is based on a well-known steepest descent method combining with nonlinear programming, which is realized by equivalent RC circuits composed of ABMs (analog behavior models) of Spice. The optimum parameters are given by the equilibrium points of the transient analysis. We show our Spice-oriented optimization algorithm using the sensitivity circuits in section 2, and the interesting illustrative examples are shown in section 5.

section

1. Introduction

Amplifiers are widely used as the building blocks of many analog circuits [1-4]. There are many kinds of designing items such as the maximum gain, low power consumption, minimum distortion and so on. We consider here a design problem for attaining both the maximum gains and the lower consumptions of amplifiers. These circuits are realized by setting suitable bias voltages of transistors and/or choosing suitable sizes (length, width) of MOSFETs, and the resistive values. Traditionally, these optimization parameters have been found by trial and error methods with Spice simulations and the experimental knowledge of the designers. However, it is really time-consuming for the circuits containing a large number of optimization parameters [6,10]. Therefore, we propose here a simple fully Spice-oriented steepest descent optimization algorithm combining with nonlinear programming. Firstly, we define the *objective function* to be minimized as follow;

$$\Phi(\mathbf{x},\mathbf{p}), \quad \mathbf{x}\in R^n, \quad \mathbf{p}\in R^k \tag{1}$$

where
$\mathbf{x}$: circuit variables such as voltages and currents.
$\mathbf{p}$: optimization parameters such as bias voltages, resistor's values and the dimensions of MOSFETs W[width, μm] and L [length, μm] and so on.

Our optimization technique based on the steepest descent algorithm is realized by the equivalent RC circuits, whose input currents are obtained by the sensitivity circuits [8] and the deviation circuits. The gradient direction for attaining the maximum gain is given by

$$\frac{dp_i}{ds} = -\frac{dS_v(\mathbf{p})}{dp_i}, \quad i=1,2,\ldots,k, \tag{2.1}$$

where $S(\mathbf{p})$ is the gain, and p_i is a optimization parameter. Unfortunately, it is impossible directly to evaluate $\frac{dS(\mathbf{p})}{dp_i}$ from the sensitivity analysis, so that we introduce the *numerical differentiation* as follows;

$$\frac{dp_i}{ds} = -\frac{S_{v,i}(\mathbf{p}+\Delta\mathbf{p}) - S_v(\mathbf{p})}{\Delta p_i}, \quad i=1,2,\ldots,k,$$
$$\Delta\mathbf{p} = (0,0,\ldots,\Delta p_i,\ldots,0)^T \tag{2.2}$$

with sufficiently small $\Delta\mathbf{p}$. Replacing the auxiliary variable "s" by time "t", our descent algorithm can be realized by the equivalent nonlinear RC circuits, and the optimum parameters can be found by the equilibrium point of the transient analysis. To design low power circuits, we need further to modify the algorithm (2.2) which is shown in section 2.2.

2. Sensitivity analysis and Spice-oriented optimization algorithm

2.1 Sensitivity analysis: The steepest descent method is the most basic optimization approach, where the gradient direction is decided by solutions of the sensitivity circuit. Let us derive the sensitivity circuit via tableau approach [8]. The *tableau equation* is given by;

$$\begin{bmatrix} \mathbf{K}_i & \mathbf{K}_v & \mathbf{0} \\ \mathbf{0} & \mathbf{1} & -\mathbf{A}^T \\ \mathbf{A} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{i} \\ \mathbf{v} \\ \mathbf{v}_n \end{bmatrix} - \begin{bmatrix} \mathbf{g}(\mathbf{v},\mathbf{i}) \\ \mathbf{E} \\ \mathbf{AJ} \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{3}$$

The first row is the Ohm's law where $bfK_i, \mathbf{K}_v$ consist of 1 and 0 elements, the second and third rows are Kirchhoff's voltage and current laws, respectively. $\mathbf{A}$ is the incidence matrix. $\mathbf{E}$ and $\mathbf{J}$ show the voltage and current sources. Now, define the *sensitivity* as follow;
Sensitivity:

$$S_{k,i} \equiv \lim_{\Delta p_i \to 0} \frac{\Delta x_k}{\Delta p_i} \tag{4}$$

We can derive the sensitivity tableau equation as follows;

$$\begin{bmatrix} \mathbf{K}_i & \mathbf{K}_v & \mathbf{0} \\ \mathbf{0} & \mathbf{1} & -\mathbf{A}^T \\ \mathbf{A} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{S}_{i,p_i} \\ \mathbf{S}_{v,p_i} \\ \mathbf{S}_{v_n,p_i} \end{bmatrix} - \begin{bmatrix} \frac{\partial \mathbf{g}(\mathbf{v},\mathbf{i})}{\partial \mathbf{v}}\Big|_{\mathbf{v}_0,\mathbf{i}_0} \mathbf{S}_{v,p_i} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix}$$
$$- \begin{bmatrix} \frac{\partial \mathbf{g}(\mathbf{v},\mathbf{i})}{\partial \mathbf{i}}\Big|_{\mathbf{v}_0,\mathbf{i}_0} \mathbf{S}_{i,p_i} \\ \delta(i) \\ \mathbf{A}\delta(i) \end{bmatrix} = \begin{bmatrix} \frac{\partial \mathbf{g}(\mathbf{v},\mathbf{i})}{\partial \mathbf{p}}\Big|_{\mathbf{v}_0,\mathbf{i}_0} \delta(i) \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{5}$$

where $\delta(i)$ means a delta function satisfying

$$\delta(i) = \begin{matrix} 1 & 2 & \ldots & i & \ldots & k \\ [0, & 0, & \ldots, & 1 & \ldots, & 0]^T \end{matrix}$$

Thus, we can develop the sensitivity circuit for any p_i parameter. Observe that the circuit configuration is equal to the original except for the nonlinear elements being replaced by the linear incremental resistors at the operating points $\mathbf{V}_0, \mathbf{I}_0$. Now, we summarize the algorithm for deriving the sensitivity circuit.

1. When one voltage source is chosen as an optimization parameter, the voltage is set to "1[V]". The other voltage sources are removed by the short-circuits.
2. When one current source is chosen as an optimization parameter, the current is set to "1[A]". The other current sources are removed by the open-circuits.
3. When resistor is chosen as an optimum parameter, it is replaced by the linear incremental resistor with the controlled source $\frac{\partial \mathbf{g}(\mathbf{v},\mathbf{i})}{\partial \mathbf{p}}\Big|_{\mathbf{v}_0,\mathbf{i}_0}\delta(i)$. Other resistors are only replaced by the incremental resistors.

Example 1: Now, consider a simple example nonlinear circuit shown in Fig.1(a), where the nonlinear resistor is

$$i = c_1 v + c_3 v^3.$$

Let us calculate the gain $S_v = dv/dE$. For the optimum parameter E, we have the sensitivity circuit shown by Fig.1(b).

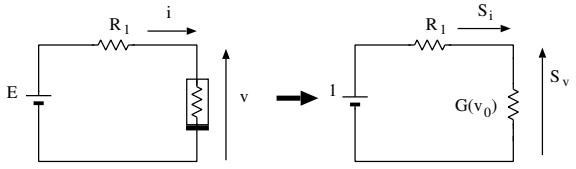

Fig.1 (a) Simple nonlinear resistive circuit, (b) the sensitivity circuit for the optimization parameter E.

The sensitivity is given by

$$S_v = \frac{1/G(v_0)}{R_1 + 1/G(v_0)} = \frac{1}{1 + R_1 G(v_0)}, \quad \text{for} \quad G(v_0) = c_1 + 3c_3 v_0^2$$

where v_0 is the voltage of nonlinear resistor in Fig.1(a).

2.2 Spice-oriented optimization technique: Now, consider optimization problems for attaining both the DC maximum gain and the low power consumption of amplifier. In this case, the steepest descent method for attaining the maximum gain given by (2.2) is modified as follows;

$$\frac{dp_i}{ds} = K(I_S - I_i(\mathbf{p}+\Delta\mathbf{p})) - \frac{S_{v,i}(\mathbf{p}+\Delta\mathbf{p}) - S_v(\mathbf{p})}{\Delta p_i} \quad (6)$$

$$K = \begin{cases} 0 & : \ I_S > I_i \\ A & : \ I_S \le I_i \ \text{ for sufficiently large } A \end{cases}$$

$$\Delta\mathbf{p} = (0, 0, \ldots, \Delta p_i, \ldots, 0)^T$$

where I_S is the assigned current of the sources, which should be set smaller value for the design of low consumption circuits. In this case, the solution curve of (6) will move to the maximum point during $I_S > I_i$. When the curve has reached to the hyper-plane $I_i = I_S$, it will moves on the plane and search the maximum point on the plane if we choose a sufficiently large constant A. Thus, we can find the point satisfying both the maximum gain and the low power consumption. Replacing the variable "s" by time "t' in (6), it is realized by RC circuit shown in Fig.2.

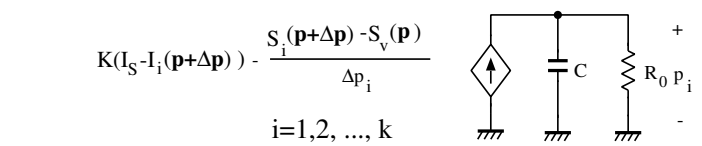

Fig.2 A circuit configuration for attaining both the maximum gain and the low power consumption.

The controlled current sources in the figure $\{\ S_{v,i}(\mathbf{p}+\Delta\mathbf{p}), I_i(\mathbf{p}+\Delta\mathbf{p}),\ i = 1, 2, \ldots, k\ \}$ are obtained from the k sensitivity circuits and the small deviation $\Delta\mathbf{p}$ circuits, respectively. Thus, the optimization parameters satisfying both the maximum gain and the low power consumption can be found at the equilibrium points of the transient analysis of (6). Note that although C's in Fig. 2 are set equal to "1" in (6), the convergence ratio will be largely increased by choosing the smaller values. R_0's are sufficient large dummy resistances to avoid C-J cut-set.

3. Sensitivity modules of MOSFETs and bipolar transistors

Now, let us develop the sensitivity modules of MOSFETs and bipolar transistors. Once these modules are stored in our computer library as the packages, we can easily formulate the sensitivity circuits.

3.1 Sensitivity module of MOSFET: We consider Shichman-Hodges model [1-4] of nMOS in Fig.3(a);

1. **Linear region**$(v_{GS} > v_T,\ 0 < v_{DS} < v_{GS} - v_T)$

$$i_D = \frac{k_n W}{L}\left[(v_{GS} - v_T) - \frac{v_{DS}}{2}\right] v_{DS}(1 + \lambda v_{DS}) \quad (7.1)$$

2. **Saturation region**$(v_{GS} > v_T,\ v_{DS} \ge v_{GS} - v_T)$

$$i_D = \frac{k_n W}{2L}(v_{GS} - v_T)^2(1 + \lambda v_{DS}) \quad (7.2)$$

where the threshold voltage is given by

$$v_t = v_{T0} + \gamma\left(\sqrt{\phi - v_{BS}} - \sqrt{\phi}\right), \quad (7.3)$$

where W and L are the width and length. For simplicity, we rewrite (7) in the following form;

$$i_D = \hat{i}_D(v_{GS}, v_{DS}, v_{BS}, W, L) \quad (8)$$

Then, we have the following variational equation;

$$\Delta i_D = \frac{\partial \hat{i}_D}{\partial v_{GS}}\Delta v_{GS} + \frac{\partial \hat{i}_D}{\partial v_{DS}}\Delta v_{DS} + \frac{\partial \hat{i}_D}{\partial v_{BS}}\Delta v_{BS} + \frac{\partial \hat{i}_D}{\partial W}\Delta W + \frac{\partial \hat{i}_D}{\partial L}\Delta L \quad (9)$$

Therefore, the sensitivity variables are given for each optimization parameter p_i

$$S_{i_D,pi} = \frac{\partial \hat{i}_D}{\partial v_{GS}} S_{v_{pi,GS}} + \frac{\partial \hat{i}_D}{\partial v_{DS}} S_{v_{pi,DS}} + \frac{\partial \hat{i}_D}{\partial v_{BS}} S_{v_{pi,BS}} + \frac{\partial \hat{i}_D}{\partial W}\delta(p_i, W) + \frac{\partial \hat{i}_D}{\partial L}\delta(p_i, L) \quad (10)$$

where δ means

$$\delta(x_1, x_2) = \begin{cases} 1 & \text{for } x_1 = x_2 \\ 0 & \text{for } x_2 \ne x_2 \end{cases}$$

Thus, we have the MOSFET module shown in Fig.3(b), where

$$G_{GS} = \frac{\partial \hat{i}_D}{\partial v_{GS}},\ G_{DS} = \frac{\partial \hat{i}_D}{\partial v_{DS}},\ G_{BS} = \frac{\partial \hat{i}_D}{\partial v_{BS}}$$

$$S_{i_D} = \frac{\partial \hat{i}_D}{\partial W}\delta(p_i, W) + \frac{\partial \hat{i}_D}{\partial L}\delta(p_i, L).$$

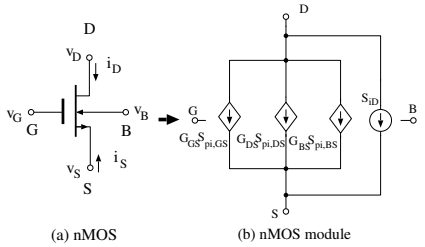

Fig.3(a) nMOS, (b) nMOS module.

3.2 Sensitivity modules of bipolar transistor: Bipolar transistor is usually modeled with Ebers-Moll model or Gummenl-Poon model [1-4]. The corrector current i_C and base current i_B are functions of v_{BE} and v_{BC} as follows;

$$\left.\begin{array}{l} i_C = \hat{i}_C(v_{BE}, v_{BC}) \\ i_B = \hat{i}_B(v_{BE}, v_{BC}) \end{array}\right\} \tag{11}$$

Therefore, the sensitivities for optimization parameters p_i are given by

$$\left.\begin{array}{rcl} S_{i_C,p_i} & = & \frac{\partial \hat{i}_C}{\partial v_{BE}} \frac{\partial v_{BE}}{\partial p_i} + \frac{\partial \hat{i}_C}{\partial v_{BC}} \frac{\partial v_{BC}}{\partial p_i} \\ & \equiv & G_{i_C,v_{BE}} S_{v_{pi},BE} + G_{i_C,v_{BC}} S_{v_{pi},BC} \\ S_{i_B,p_i} & = & \frac{\partial \hat{i}_B}{\partial v_{BE}} \frac{\partial v_{BE}}{\partial p_i} + \frac{\partial \hat{i}_B}{\partial v_{BC}} \frac{\partial v_{BC}}{\partial p_i} \\ & \equiv & G_{i_B,v_{BE}} S_{v_{pi},BE} + G_{i_B,v_{BC}} S_{v_{pi},BC} \end{array}\right\} \tag{12}$$

Thus, the sensitivity module of NPN bipolar is given by Fig.4(c)[1].

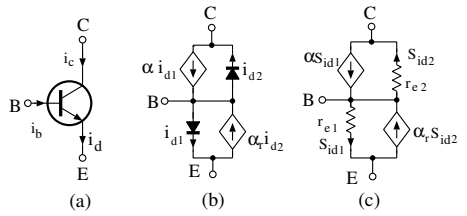

Fig.4(a) NPN bipolar transistor, (b) Ebers-Moll model, (c) sensitivity modue of transistor module.

4. Resistive models of RC circuits

The left hand side of our Spice-oriented optimization method shown in Fig.2 is composed of the controlled-current sources which are obtained from the small deviations Δp_i circuits and the sensitivity circuits. Both circuits are resistive. Therefore, our optimization method should not contain any dynamical elements such as capacitors and inductors. On the other hand, many kinds of amplifiers may consist of capacitors so that we need approximately to transform them into the resistive models. We propose two types modeling as follows;

1. The model 1 is replacing each capacitor with the impedance
$$Z_C = |\frac{1}{j\omega C} = \frac{1}{\omega C} \tag{13.1}$$
2. The model 2 is replacing the series and parallel RC circuits with the corresponding impedances as follows;
$$Z_{RC,S} = \sqrt{R^2 + \frac{1}{\omega^2 C^2}},\ Z_{RC,P} = \frac{R}{\sqrt{1+\omega^2 C^2 R^2}} \tag{13.2}$$

Example 2: Consider a simple circuit containing a series and a parallel RC circuits as shown in Fig.5(a).

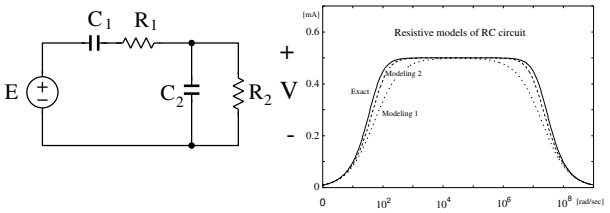

Fig.5(a) A simple RC circuit, (b) Frequency response curves. $R_1 = R_2 = 10[k\Omega],\ C_1 = 1[\mu F],\ C_2 = 10[pF]$

[1]The method can be also applied to Gummel-Poon model of bipolar transistor.

All the frequency response curves by models 1 and 2 are almost same except for the cut-off frequency regions. Note that even if the model 2 is complicate model compared with model 1, the response curve with model 2 is much more exact than that of model 1[2].

5. Illustrative examples

5.1 CMOS two-stage amplifier [4]: Consider a two-stage amplifier as shown in Fig.6(a). Let us design it satisfying both the maximum gain and low power consumption.

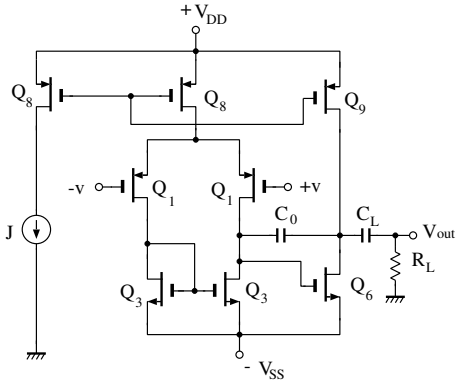

Fig.6(a) Two stage CMOS amplifier.
$V_{DD} = 2.5[V],\ \ V_{SS} = -2.5[V]$, Frequency $=1[MHz]$
$C_0 = 10[nF],\ C_L = 1[nF]$

For the MOS and the circuit parameters from ref.[4]:

$K_p = 19.344[\mu A]$,	$pV_{T0} = -0.8311[V]$,	$p\lambda = 0.1$
$pW9 = 10[\mu m]$,	$pW8 = 50[\mu m]$,	$pW1 = 50[\mu m]$,
$K_n = 74.209[\mu A]$	$nV_{T0} = 0.6081[V]$,	$n\lambda = 0.2$
$nW3 = 1[\mu m]$	$nW6 = 3[\mu m]$,	$pL = nL = 0.5[\mu m]$
$J = 90[\mu A]$		

We get Gain=-1.956 from the transient analysis of Spice. Next, we design the CMOS circuit with the initial conditions as follows; $pW9 = 2[\mu m],\ pW8 = pW1 = nW6 = 5[\mu m]$ $nW3 = 10[\mu m],\ J_0 = 5[\mu A]$ and $C = 0.01,\ \ R_0 = 1000[k\Omega]$ in the steepest descent method in Fig.2. We have restricted the following 6 optimization parameters as follows;

$$1.5[\mu m] < pW9, pW8, pW1, nW3, nW6 < 60[\mu m]$$
$$5[\mu A] < I_{in} < 200[\mu A]$$

Then, we have obtained the results of Table 1.

Table 1 Simulation results.

No	A	I_S (μA)	I_{in} (μA)	J (μA)	$Gain_D$	$Gain_T$	R_L ($k\Omega$)
1	-	-	120.1	55.3	-19.6	-19.6	-
2	10^4	50	52.4	23.3	-19.1	-20.1	-
	10^5	50	49.8	22.5	-20.4	-21.5	-
	10^6	50	49.6	22.4	-20.4	-21.5	-
3	10^6	40	39.6	17.7	-3.30	-3.33	10
	10^6	40	39.7	17.7	-13.1	-13.3	100
	10^6	40	39.7	17.7	-18.7	-19.6	1000

where A is a sufficiently large constant in (6), and the computational time was around 225-230[sec]. Firstly, we have assigned I_S which is the current from bias V_{DD}. It is equal to sum of the current source J and the current to V_{SS}. I_{in}, $Gain_D$ are the current and gain obtained by

[2]Parasitic capacitors in transistors can not be neglected in the high frequency. We recommend to use model 1 even if it is erroneous, because the circuit configurations are complicate.

our optimization, and $Gain_T$ is the gain estimated by the transient analysis of Fig.6(a). We found interesting results as follows;

1. No.1 is the optimization result for only attaining the maximum gain without no restrictions. We have the following sizes;

   $$pW8 = pW1 = nW3 = 60[\mu m],\ pW9 = nW6 = 1.5[\mu m]$$

   where we have set $pL = nL = 0.5[\mu m]$ for all the MOSFETs. Then, the input current $I_{in} = 120.1[\mu A]$ is large. Note that this kind of simulation is called *nonlinear programming [5].*

2. No.2 is the results for attaining both the maximum gain and low power consumption ($I_S = 50[\mu A]$) without coupling capacitor ($C_L,\ R_L$), where we set A from 10^4 to 10^6 in (6). For $A = 10^4$, we had $pW8 = 17.82[\mu m]$ and $I_{in} = 52.39[muA]$ which is different from the assigned current $I_S = 50[\mu A]$. Thus, we can conclude that we need to choose larger $A > 10^5$.

3. No.3 is the results for the load impedances, where we used the model 1 in (13.1) for the capacitor C_L and C_0;

   $$Z_C = |\frac{1}{j\omega C_C}| = 159.$$

   Although the gains are largely changed by the load resistance R_L, they are almost equal to the results from the transient analysis.

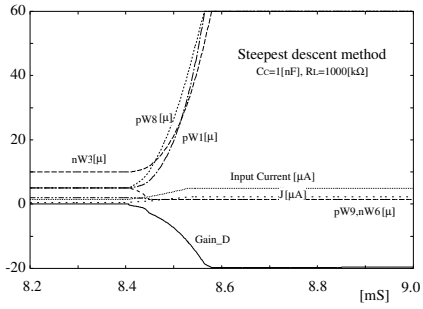

Fig.6(b) Optimization of two stage CMOS amplifier. $R_L = 1000[k\Omega],\ C_L = 1[nF],$ Frequency $=1[MHz]$

5.2 Operational amplifier [4]: Consider an operational amplifier shown in Fig.7(a). The maximum gain is attained by choosing suitable resistors $R_1 - R_5$ in the figure.

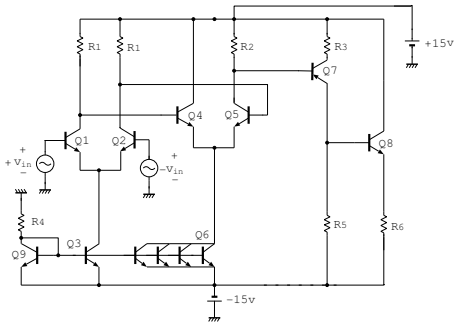

Fig.7(a) Bipolar operational amplifier.

For parameter in ref[4],

$$R_1 = 10[k\Omega],\ R_2 = 3[k\Omega], R_1 = 2.3[k\Omega], R_4 = 28[k\Omega],$$
$$R_5 = 15.7[k\Omega], R_6 = 3[k\Omega]$$

We had the gain of $77.80[dB]$.
In order to attain the maximum gain, we have restricted the optimization parameters as follows;

$$10[k\Omega] < R_1 < 55[k\Omega],\ 1[k\Omega] < R_2 < 6[k\Omega],$$
$$0.5[k\Omega] < R_3 < 5[k\Omega],\ 40[k\Omega] < R_4 < 60[k\Omega],$$
$$10[k\Omega] < R_5 < 50[k\Omega],\ R_6 = 3[k\Omega]$$

Then, we had

$$R_1 = 55[k\Omega],\ R_2 = 1.0[k\Omega], R_1 = 0.5[k\Omega], R_4 = 40[k\Omega],$$
$$R_5 = 50[k\Omega], R_6 = 3[k\Omega]$$

whose maximum gain is equal to $87.07[dB]$. The optimization result of the steepest descent method is shown in Fig.7(b). Thus, we can design the operational amplifier having enough gain. The computation time was 36.95[sec].

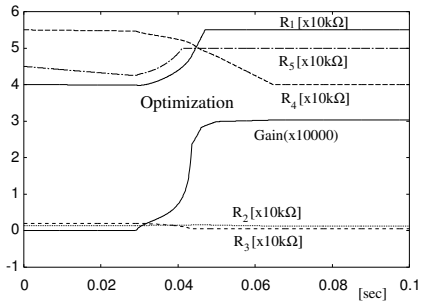

Fig.7(b) Optimization result of operational amplifier.

6. Conclusions and remarks

In this paper, we propose a Spice-oriented design algorithm of the amplifies for attaining both the maximum gain and low power consumption. The algorithm is based on the steepest descent method, which is realized by the nonlinear RC circuits with ABMs of Spice. we found that our optimization simulator is much faster than a simulator ASCO(A SPICE Circuit Optimizer) [10].

References

[1] G.Roubik, *Introduction to CMOS OP-AMPs and Comparators,* Wiley-Interscience Pub., 1999.

[2] F.Maloberti, *Analog Design for CMOS VLSI Systems,* KLuwer Academic Pub., 2001.

[3] S.M.Kang, and Y.Leblebici, *CMOSW Digital Integrated Circuits: Analysis and Design,* McGraw-Hill Co.Inc., 1996.

[4] A.S.Sedra and K.C.Smith, *Microelectronic Circuits,* Oxford Univ. Press, 2004.

[5] J.A.Snyman *Practical Mathematical Optimization: An Introduction to Basic Optimization Theory and Classical and New Gradient-Based Algorithm,* Springer, 2005.

[6] K.Ono, K.Saeki,Y.Sekine,"A design of an operational amplifier with high DC gain," *The Papers of Tech. meeting on Electronic Circuits, IEE Japan,* ECT-04-99, pp.1-5, 2004.

[7] J.Guo, T.Nishi and N. Takahashi, "A method for solving optimization problems with equality constraints by using Spice program," *IEICE Trans*, vol.E86-A, no.9,pp.2325-2332, 2003.

[8] L.O.Chua and P-M Lin, *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques,* Prentice-Hall, 1975.

[9] MicroSim: *PSpice A/D circuit Analysis User's Guides,* MicroSim Co. 1995.

[10] http://asco.sourceforge.net/