2006 RISP International Workshop
on Nonlinear Circuits and Signal Processing (NCSP'06)
Waikiki Beach Marriott, Honolulu,
Hawaii, USA, March 3-5, 2006

Frequency Domain Analysis of CMOS Amplifiers Containing Parasitic Capacitors

Yousuke Taniguchi†, Yoshihiro Yamagami†, Yoshifumi Nishio† and Akio Ushida‡

†Tokushima University
2-1 Minami-Josanjima, Tokushima, Japan
Phone:+81-88-656-7470/FAX:+81-88-656-7471
Email: yousuke@ee.tokushima-u.ac.jp

‡Tokushima Bunri University
1314-1 Shido, Kagawa, Japan
Phone:+81-87-894-5111/FAX:+81-87-894-4201
Email: ushida@fe.bunri-u.ac.jp

Abstract

Distortion analysis of nonlinear circuits is very important for designing analog integrated circuits and/or communication systems. We consider here the frequency-domain analysis of CMOS operational amplifiers in the high frequency domain. In this case, the parasitic capacitors among source, drain, gate and substrate of MOSFETs give large effects to the characteristics. In this study, we propose a harmonic balance method to solve the frequency response curves. It is known that the determining equations are given by the analytical functions only when the nonlinear characteristics are given by polynomial functions. Unfortunately, many nonlinear devices are modeled by the use of many kinds of special functions and piecewise continuous functions, so that we cannot apply analytical harmonic balance methods. Therefore, we develop the Fourier Transfer Circuit Models (FTCM) using ABMs (Analog Behavior Models) of Spice which carries out the Fourier transformation of MOSFETs containing nonlinear parasitic capacitors.

1. Introduction

Recently, owing to the rapid progress of integrated circuit technologies, high frequency CMOS amplifiers have been frequently used in high performance RF communication systems [1-3]. On the other hand, the characteristics of MOSFETs have strong nonlinearity. Especially, the parasitic capacitors in the high frequency give large effects to the characteristics [2,4-6].

There are two techniques in the frequency domain analysis of nonlinear circuits; namely, Volterra series [4-7] and harmonic balance methods [8-10]. The Volterra series methods can be usually applied to weak nonlinear circuits. In this case, the characteristics of nonlinear elements should be described by the power series expansions in the vicinity of the driving point. The task is not easy for nonlinear electronic circuits such as bipolar transistors and MOSFETs [6]. On the other hand, the harmonic balance methods are usefully applied to the circuits containing any kind of nonlinear devices. However, it is also not easy to derive the circuit equations and the determining equations for the harmonic balance method [8].

In this paper, we propose a new Spice-oriented harmonic balance method solving the frequency response curves of CMOS amplifiers [10-11]. Firstly, we develop the "packaged device modules" executing the Fourier expansions of MOSFETs and bipolar transistors. Then, the determining equations are given in the form of coupled equivalent circuits. The frequency response curves can be calculated by DC analysis of Spice. Thus, our simulators are really user-friendly.

We show the idea of the proposed FTCM in Section 2, and the application to MOSFET in Section 3. The illustrative examples are introduced in Section 4.

2. Fourier transfer circuit model

Analog integrated circuits are usually composed of many kinds of nonlinear devices such as diodes, bipolar transistors and MOSFETs, whose Spice models are described by the special functions such as exponential, square-root, piecewise continuous functions and so on [12]. For these devices, the Fourier coefficients cannot be described in the analytical forms. Therefore, using ABMs of Spice [13], we will realize the equivalent circuits executing the Fourier expansions in the harmonic balance methods. Now, consider a nonlinear function described by

$$i = \hat{g}(v(t)). \tag{1}$$

Assume that the input and output waveforms are described as follows;

$$\left.\begin{aligned} v(t) &= V_0 + \sum_{k=1}^{K}(V_{2k-1}\cos k\omega t + V_{2k}\sin k\omega t) \\ i(t) &= I_0 + \sum_{k=1}^{K}(I_{2k-1}\cos k\omega t + I_{2k}\sin k\omega t) \end{aligned}\right\} \tag{2}$$

where K shows the highest harmonic component in our analysis. Here, applying the discrete Fourier transformation to (2), the Fourier coefficients of the output current are described as follows;

$$\left.\begin{array}{l} I_0 = \frac{1}{T}\int_0^T \hat{g}(v(t))dt \\ I_{2k-1} = \frac{2}{T}\int_0^T \hat{g}(v(t))\cos k\omega t dt \\ I_{2k} = \frac{2}{T}\int_0^T \hat{g}(v(t))\sin k\omega t dt \\ k = 1, 2, \cdots, K \end{array}\right\}. \quad (3)$$

Next, let us apply the following trapezoidal integration formula to (3);

$$\int_a^b f(x)dx = \frac{h}{2}(f_0 + f_n) + h(f_1 + f_2 + \cdots + f_{n-1}) \quad (4)$$

where the step size of the integration is $h = (a-b)/n$. Then, the truncation error is given by $f^{(2)}h^2/12n$, where $^{(2)}$ shows the second derivative. We show that (3) with (4) can be realized by the equivalent circuit model.

The blocks in Fig. 1 are constructed by the ABMs of Spice, where the interval $[0, 2\pi]$ of the integration is divided by 2K equal divisions. The value of $\theta_k = 2\pi/2K$ is obtained by the node voltage at the Kth resistor in the resistive circuit.

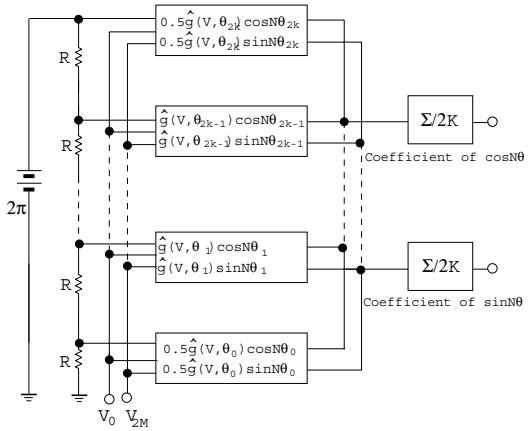


Figure 1: Fourier transfer circuit model.

To investigate the accuracy of our FTCM, we calculate the following Fourier expansion:

$$e^{x\cos\theta} = I_0(x) + I_1(x)\cos\theta + I_2(x)\cos 2\theta + \cdots. \quad (5)$$

The simulation result for $h = 2\pi/20$ in Fig. 1 is $I_1(10) = 2761$ at N=1, x=10 which is exactly equal to the value from the table of Bessel function. Thus, we found that the FTCM can get the sufficiently exact solution even with $2K$=10 to 20 divisions of the interval 2π.

3. FTCM of MOSFET

Now, consider FTCM of MOSFET. The drain current of nMOS is given by the Schichman-Hodges model as follows [1-2]:

(a) Linear region

$(V_{GS} > V_T,\ \ 0 < V_{DS} < V_{GS} - V_T)$

$$I_D = \frac{k'W}{L}\Big[(V_{GS} - V_T) - \frac{V_{DS}}{2}\Big]V_{DS}(1 + \lambda V_{DS}). \quad (6)$$

(b) Saturation region

$(V_{GS} > V_T,\ \ V_{DS} \geq V_{GS} - V_T)$:

$$I_D = \frac{k'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}). \quad (7)$$

The threshold voltage is given by

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}). \quad (8)$$

The parasitic capacitors are shown in Fig. 2. When the gate voltage is less than the threshold voltage, the channel does not appear. However, in the linear region, the channel equally spread between the source and drain terminals, so that C_{GD} and C_{GS} contain equal $\frac{1}{2}C_{ox}WL$. On the other hand, in the saturation region, the channel spread like as Fig. 2. C_{GD} contains $\frac{1}{3}C_{ox}WL$ and C_{GS} does $\frac{2}{3}C_{ox}WL$. They have also depletion capacitances given in (9) between substrates. Thus, the characteristics of parasitic capacitors are given in Table 1 [12]. The circuit model in high frequency is shown in Fig. 3.

$$C_{SB} = \frac{A_S C_{j0}}{[1 + (V_{SB}/\phi)]^m},\ \ m \simeq 0.5. \quad (9)$$

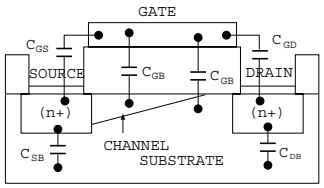


Figure 2: Parasitic capacitors for nMOS.

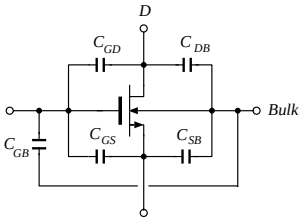


Figure 3: MOSFET in the high frequency.

Table 1: Terminal capacitances of a MOSFET.

	Regions	
Parasitic capacitors	Linear region	Saturation region
C_{GD}	$C_{ox}WL_D + \frac{1}{2}C_{ox}WL$	$C_{ox}WL_D$
C_{GS}	$C_{ox}WL_D + \frac{1}{2}C_{ox}WL$	$C_{ox}WL_D + \frac{2}{3}C_{ox}WL$
C_{BG}	0	$\frac{\frac{1}{3}WLC_{ox}C_{pn}(V_{DB})}{C_{ox}+C_{pn}(V_{DB})}$
C_{BD}	$A_D C_{pn}(V_{DB})$ $+\frac{1}{2}WLC_{pn}(V_{DB})$	$A_D C_{pn}(V_{DB})$
C_{BS}	$A_S C_{pn}(V_{SB})$ $+\frac{1}{2}WLC_{pn}(V_{SB})$	$A_S C_{pn}(V_{SB})$ $+\frac{2}{3}WLC_{pn}(V_{SB})$

Note that the characteristics of the nonlinear parasitic capacitors in Table 1 are piecewise discontinuous functions. The results obtained using the paramerter values given in Table 2 are shown in Figs. 4 and 5.

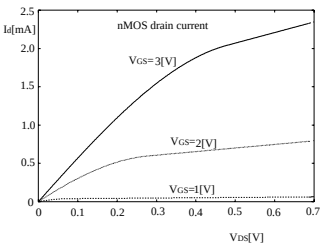


Figure 4: Drain current of nMOS.

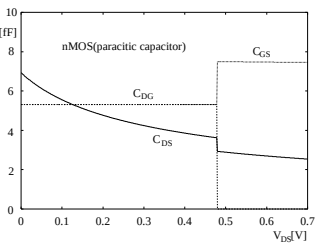


Figure 5: Parasitic capacitors of nMOS.

Observe that the parasitic capacitors give large effects in the high frequency, though their order is $10^{-15}F$.

Table 2: MOS parameter [13] (MKS system).

Mark	pMOS	nMOS
L	1.2×10^{-6}	1.2×10^{-6}
W	7.8×10^{-6}	7.8×10^{-6}
L_D	900.1×10^{-12}	900.1×10^{-12}
pV_{T0}, nV_{T0}	-0.8311	0.6081
k_p, K_n	19.34×10^{-6}	74.21×10^{-6}
λ	0.1	0.2
$p\gamma, \gamma$	0.3046	0.6166
C_{j0}	259.97×10^{-6}	280.65×10^{-6}

Other parameters :
$A_S = A_D = 20 \times 10^{-12}$, $t_{ox} = 30.4 \times 10^{-9}$, $\phi = 0.7$
$C_{ox} = 1.135 \times 10^{-3}$.

Now, let us derive the FTCM of MOSFET. We assume that the terminal voltage is given by equation (10).

$$v_t(t) = V_{t,0} + \sum_{k=1}^{K}(V_{t,2k-1}\cos k\omega t + V_{t,2k}\sin k\omega t) \quad (10)$$

$$t = D, G, S, B.$$

Here, D,G,S,B correspond to the terminal shown in Fig. 3. First, we assume $\theta = \omega t$, and divide period 2π in equal step size $[\theta = 0, 2\pi/K, 4\pi/K, \ldots, 2\pi]$, and calculate the current at each point. And we apply a trapezoidal integration formula of equation (4) instead of equation (3) whose calculations are carried out by Fig. 1 using Spice.

Thus, the Fourier coefficients are calculated as follows:

$$i_t(t) = I_{t,0} + \sum_{k=1}^{K}(I_{t,2k-1}\cos k\omega t + I_{t,2k}\sin k\omega t) \quad (11)$$

$$t = D, G, S, B.$$

In the same way, the response of capacitor charges are also expanded into the Fourier series as follows;

$$q_p(t) = Q_{p,0} + \sum_{k=1}^{K}(Q_{p,2k-1}\cos k\omega t + Q_{p,2k}\sin k\omega t) \quad (12)$$

$$p = DS, GS, DG, DB, GB, SB.$$

We differentiate equation (12) with respect to time, the current are given as follows:

$$i_p(t) = \sum_{k=1}^{K} k\omega(-Q_{p,2k-1}\sin k\omega t + Q_{p,2k}\cos k\omega t). \quad (13)$$

Comparing each harmonic component, we can obtain equivalent circuits corresponding to determining equations. If we assume that the numbers of harmonic component is K, the numbers of subcircuit are $2K + 1$. They are combined with controlled sources in each other [10].

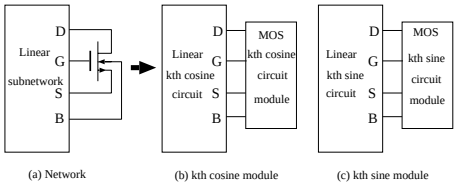


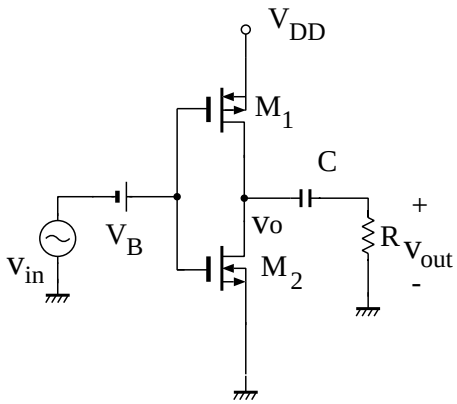
Figure 6: Sine-Cosine circuits using MOS modules for kth harmoninc components.

4. Fourier analysis of CMOS differential amplifiers

4.1 CMOS amplifier

Let us calculate the frequency response curves of differential amplifiers, whose MOSFET parameters are given by Table 2. In our simulations, we consider until the 3rd harmonic component.

First, we consider the amplifier circuit using the characteristics of a CMOS inverter circuit shown by Fig. 7.



$V_{DD} = 3[V]$, $V_B = 1.2[V]$, $C = 10[pF]$, $R = 100[k\Omega]$.

Figure 7: CMOS amplifier circuit.

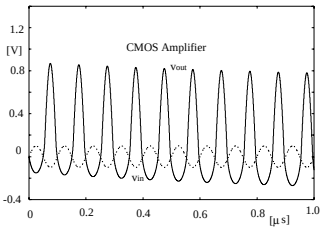


Figure 8: transient response of the CMOS amplifier.

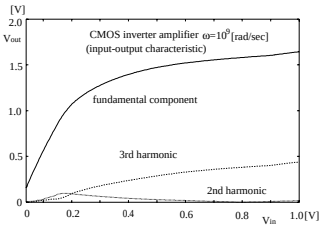


Figure 9: Input and output characteristics of the CMOS inverter amplifier.

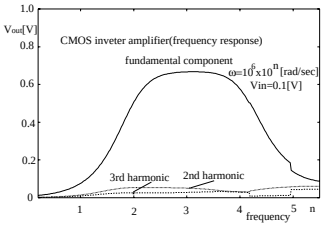


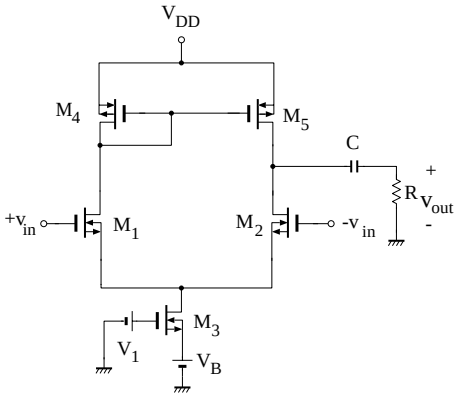
Figure 10: Frequency responses of CMOS inverter amplifier.

The output voltage waveform $v_{out}(t)$ to the input $v_{in}(t) = 0.1\sin 10^7 t$ is shown by Fig. 8. The output waveform is

largely distorted. Next, changing the amplitude of the input voltage from $V_{in} = 0$ to 1, the responses of the output waveforms and the higher harmonic components are shown by Fig. 9. Next, we calculated the frequency response curves, where the frequency is changed by $\omega = 10^{6+n}$ for a variable n, and assume the input by $V_{in} = 0.1[V]$. Thus, we can obtain the frequency response curves shown by Fig. 10.

4.2 Differential amplifier [2]

Next, we consider an n-channel differential amplifier given by Fig. 11. The results in this case are shown in Figs. 12 and 13.



$V_{DD} = V_B = 3[V],\ V_1 = 2[V],\ C = 10[pF],\ R = 100[k\Omega]$.
Figure 11: An n-channel differential amplifier.

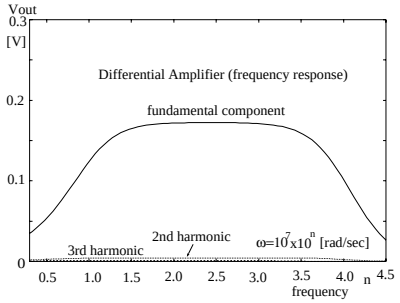


Figure 12: Frequency response curves of the differential amplifier. $V_{in} = 0.1$.

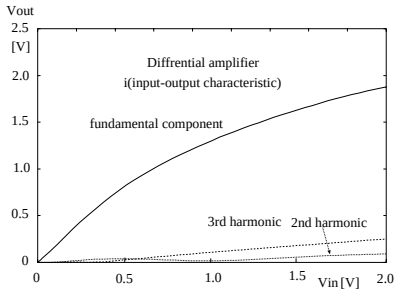


Figure 13: Input and output characteristics of the differential amplifier. $\omega = 10^9[rad/sec]$.

The results in Fig. 12 are the frequency response curves for the input [$V_{in} = 0.1[V]$]. Next, we calculated the input and the output characteristics at $\omega = 10^9[rad/sec]$. The results are shown by Fig. 13.

5. Conclusions and remarks

In this study, the nonlinear devices such as bipolar transistors and MOSFETs were transformed into the modules executing the Fourier transformations. Using these device modules, the nonlinear circuit was transformed into the Fourier circuit corresponding to the determining equations of the harmonic balance method. They were solved with the DC analysis of Spice.

References

[1] S.M.Kang, and Y.Leblebici, *CMOSW Digital Integrated Circuits: Analysis and Design*, McGraw-Hill Co.Inc., 1996.

[2] G.Roubik, *Introduction to CMOS OP-AMPs and Comparators*, Wiley-Interscience Pub., 1999.

[3] F.Maloberti, *Analog Design for CMOS VLSI Systems*, KLuwer Academic Pub., 2001.

[4] P.Wambacq and W.Sansen, *Distortion Analysis of Analog Integrated Circuits*, Kluwer Academic Pub., 1998.

[5] D.Leenaerts, J.V.Tang, and C.Vaucher, *Circuit Design for RF Transceivers*, KLuwer Academic Pub., 2001.

[6] A.Bauer and W.Schwarz, "Algorithms for the efficient computation of Volterra Kernels in the behavior analysis of periodically excited nonlinear dynamical circuits and systems," Proc. of NOLTA'05, pp.509-512, 2005.

[7] M.Schetzen, *The Volterra and Wiener Theorems of Nonlinear Systems*, John Wiley and Sons, 1987.

[8] K.S.Kundert, J.K.White and A.Sangiovanni-Vincentelli, *Steady-State Methods for Simulating Analog and Microwave Circuits*, Kluwer Academic Pub., 1990.

[9] A.Ushida, T.Adachi and L.O.Chua, "Steady-state analysis of nonlinear circuits based on hybrid methods," *IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications*, vol.39, no.9, pp.649-661, 1992.

[10] A.Ushida, Y.Yamagami and Y.Nishio, "Frequency responses of nonlinear networks using curve tracing algorithm,"Proc. of *ISCAS 2002*, vol.I, pp.641-644, 2002.

[11] A.Ushida, J.Kawata, Y.Yamagami and Y.Nishio, "Intermodulation analysis of nonlinear circuits using two-dimensional Fourier transformation," Proc. of NOLTA'05, pp.282-285, 2005.

[12] MicroSim: PSpice A/D Circuit Analysis User's Guides, MicroSim Co., 1995.

[13] J.E.Meyer, "MOS models and circuit simulation," *RCA Review*, Vol. 32, 1971.